TLE9183QK User Manual

Bridge Driver IC

About this document

Scope and purpose

This document includes additional information to the Data Sheet of TLE9183QK:

- ***Pin Definitions and Functions***
- ***General Failure Behavior Timing Diagrams***
- ***Phase Cut Off Activation***
- ***Self Test Mode***
- ***Register Description***
- ***Register Specification***
- ***Additional Components Recommendation***

Intended audience

This document is intended for experienced engineers who develop motor drive applications.

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1 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	*Ground* Connect this pin to ground.
2	APC	*Activation Phase Cut off Circuit* Digital output referred to 5 V. Connect this safe state output pin to the driving circuit for the phase separation FETs. Can be used for any other safe state circuit. If not used keep pin open.
3	$\overline{\text{ERR}}$	*Error Not* Digital active-low error output pin referred to VCC supply voltage. Indication for ready for configuration when high after power-up. If not used keep pin open.
4	$\overline{\text{IH1}}$	*Input High-side 1 Not* Digital active-low input pin to turn on/off high-side FET 1 referred to VCC supply voltage.
5	IL1	*Input Low-side 1* Digital active-high input pin to turn on/off low-side FET 1 referred to VCC supply voltage.
6	IL2	*Input Low-side 2* Digital active-high input pin to turn on/off low-side FET 2 referred to VCC supply voltage.
7	$\overline{\text{IH2}}$	*Input High-side 2 Not* Digital active-low input pin to turn on/off high-side FET 2 referred to VCC supply voltage.
8	$\overline{\text{IH3}}$	*Input High-side 3 Not* Digital active-low input pin to turn on/off high-side FET 3 referred to VCC supply voltage.
9	IL3	*Input Low-side 3* Digital active-high input pin to turn on/off low-side FET 3 referred to VCC supply voltage.
10	MISO	*Master In Slave Out* Digital SPI signalling output port referred to VCC supply voltage. Connect to SPI port “data input” of µC to send status information during SPI communication.
11	MOSI	*Master Out Slave In* Digital SPI signalling input port referred to VCC supply voltage. Connect to SPI port “data output” of µC to receive commands during SPI communication.
12	CSN	*Chip Select Not* Digital active-low SPI signalling input port referred to VCC supply voltage. Connect to SPI port “chip select” of µC to address the device for SPI communication.
13	CLK_SPI	*Clock Serial Peripheral Interface* Digital SPI signalling input port referred to VCC supply voltage. Connect to SPI port “clock” of µC to clock the device for SPI communication.
14	VCC	*VCC Supply Voltage* Power supply for digital I/O pins and input for VCC monitoring. Connect to I/O supply of µC.
15	VO3	*Voltage Output of CSA 3*

Pin Definitions and Functions

Pin	Symbol	Function
		Analog output of current sense amplifier 3 for shunt signal amplification referred to 5 V. Connect to analog-to-digital converter.
16	$\overline{\text{SOFF}}$	*Safe Off Not* Analog active-low input pin to turn all FETs off and to enter safe off mode. Functional independent to ENA pin.
17	ISN3	*Input Shunt Negative of CSA 3* Negative input of current sense amplifier 3 for shunt signal amplification. An external input filter is recommended. If current sense amplifier 3 is not used the pin shall be connected to GND and deactivate CSA 3 at configuration mode.
18	ISP3	*Input Shunt Positive of CSA 3* Positive input of current sense amplifier 3 for shunt signal amplification. An external input filter is recommended. If current sense amplifier 3 is not used the pin shall be connected to GND and deactivate CSA 3 at configuration mode.
19	N.C.	*Not Connected* Keep pin open and do not connect to GND
20	VDHP	*Voltage Drain High-side Power* Low reference for charge pump 2. Sense input for VDHP under- and overvoltage detections, shutdown and readout. Sense input for phase voltage feedback PFBx threshold. Sense input for short circuit detection (SCD) of all high-side FETs. (Note: Depends on configuration, bit en_vdh3. If pins VDHx are used for short circuit detection (activated via SPI) then VDHP pin is not the sense input for SCD.) Connect this pin directly (low ohmic and low inductive) to recommended common star point of the drains of the high-side FETs and buffer capacitor(s).
21	CH2	*Charge Pump 2 High* Positive terminal for pump capacitor of charge pump 2. Connect the pump capacitor as close as possible to pin.
22	CL2	*Charge Pump 2 Low* Negative terminal for pump capacitor of charge pump 2. Connect the pump capacitor as close as possible to pin.
23	N.C.	*Not Connected* Keep pin open and do not connect to GND
24	$\overline{\text{INH}}$	*Inhibit Not* Analog active-low inhibit pin. Sets device into sleep mode for low quiescent current consumption. External FETs are turned off actively before the charge pumps are turned off. Reset via inhibit requires a new configuration via SPI.
25	Vs	*Voltage Supply* Supply voltage for device. Connect to supply (battery) voltage with reverse polarity protection circuit and capacitor between pin and GND. An EMC filter is recommended.
26	N.C.	*Not Connected* Keep pin open and do not connect to GND
27	CH1	*Charge Pump 1 High* Positive terminal for pump capacitor of charge pump 1. Connect the pump capacitor as close as possible to pin.

Pin Definitions and Functions

Pin	Symbol	Function
28	CL1	*Charge Pump 1 Low* Negative terminal for pump capacitor of charge pump 1. Connect the pump capacitor as close as possible to pin.
29	CP_GND	*Charge Pump Ground* GND pin for the charge pumps. Connect this pin directly (low ohmic and low inductive) to GND.
30	CB	*Charge Pump Buffer* Buffer capacitor connection for charge pump 1. Connect the capacitor as close as possible to pin.
31	GL1	*Gate Low-side 1* Analog I/O pin to turn on/off low-side FET 1. Connect to the gate of low-side FET 1. A gate resistor is recommended.
32	SL1	*Source Low-side 1* Analog I/O pin to turn on/off low-side FET 1. Connect to the source of low-side FET 1. If transients violate maximum rating or functional range external protection circuit is required.
33	BH1	*Bootstrap High-side 1* Analog I/O pin. Positive terminal to high-side buffer capacitor 1. Connect the capacitor as close as possible to pin.
34	SH1	*Source High-side 1* Analog I/O pin to turn on/off high-side FET 1 and negative terminal to high-side buffer capacitor. Connect the capacitor as close as possible to pin and connect to the source of high-side FET 1. Connection to motor and input for phase voltage feedback circuit. If transients violate maximum rating or functional range external protection circuit is required.
35	GH1	*Gate High-side 1* Analog I/O pin to turn on/off high-side FET 1. Connect to the gate of high-side FET 1. A gate resistor is recommended.
36	VDH1	*Voltage Drain High-side 1* Sense input for short circuit detection (SCD) of high-side FET 1. (Note: Depends on configuration, bit en_vdh3. If pins VDHx are used for short circuit detection (activated via SPI) then VDHP pin is not the sense input for SCD.) Connect directly to the drain of high-side FET 1, or not connected if not configured.
37	SL2	*Source Low-side 2* Analog I/O pin to turn on/off low-side FET 2. Connect to the source of low-side FET 2. If transients violate maximum rating or functional range external protection circuit is required.
38	GL2	*Gate Low-side 2* Analog I/O pin to turn on/off low-side FET 2. Connect to the gate of low-side FET 2. A gate resistor is recommended.
39	N.C.	*Not Connected* Keep pin open and do not connect to GND
40	VDH2	*Voltage Drain High-side 2* Sense input for short circuit detection (SCD) of high-side FET 2. (Note: Depends on configuration, bit en_vdh3. If pins VDHx are used for short circuit detection (activated via SPI) then VDHP pin is not the sense input for SCD.)

Pin Definitions and Functions

Pin	Symbol	Function
		Connect directly to the drain of high-side FET 2, or not connected if not configured.
41	BH2	*Bootstrap High-side 2* Analog I/O pin. Positive terminal to high-side buffer capacitor 2. Connect the capacitor as close as possible to pin.
42	SH2	*Source High-side 2* Analog I/O pin to turn on/off high-side FET 2 and negative terminal to high-side buffer capacitor. Connect the capacitor as close as possible to pin and connect to the source of high-side FET 2. Connection to motor and input for phase voltage feedback circuit. If transients violate maximum rating or functional range external protection circuit is required.
43	GH2	*Gate High-side 2* Analog I/O pin to turn on/off high-side FET 2. Connect to the gate of high-side FET 2. A gate resistor is recommended.
44	N.C.	*Not Connected* Keep pin open and do not connect to GND
45	VDH3	*Voltage Drain High-side 3* Sense input for short circuit detection (SCD) of high-side FET 3. (Note: Depends on configuration, bit en_vdh3. If pins VDHx are used for short circuit detection (activated via SPI) then VDHP pin is not the sense input for SCD.) Connect directly to the drain of high-side FET 3, or not connected if not configured.
46	BH3	*Bootstrap High-side 3* Analog I/O pin. Positive terminal to high-side buffer capacitor 3. Connect the capacitor as close as possible to pin.
47	SH3	*Source High-side 3* Analog I/O pin to turn on/off high-side FET 3 and negative terminal to high-side buffer capacitor. Connect the capacitor as close as possible to pin and connect to the source of high-side FET 3. Connection to motor and input for phase voltage feedback circuit. If transients violate maximum rating or functional range external protection circuit is required.
48	GH3	*Gate High-side 3* Analog I/O pin to turn on/off high-side FET 3. Connect to the gate of high-side FET 3. A gate resistor is recommended.
49	SL3	*Source Low-side 3* Analog I/O pin to turn on/off low-side FET 3. Connect to the source of low-side FET 3. If transients violate maximum rating or functional range external protection circuit is required.
50	GL3	*Gate Low-side 3* Analog I/O pin to turn on/off low-side FET 3. Connect to the gate of low-side FET 3. A gate resistor is recommended.
51	GND	*Ground* Connect this pin to ground.
52	N.C.	*Not Connected* Keep pin open and do not connect to GND
53	PFB3	*Phase Voltage Feedback 3*

Pin Definitions and Functions

Pin	Symbol	Function
		Digital output pin referred to VCC supply voltage. Feedback for µC of the state of the motor connection of pin SH3 referred to voltage at VDHP. Connect to PFB 3 port to µC. If not used keep pin open.
54	PFB2	*Phase Voltage Feedback 2* Digital output pin referred to VCC supply voltage. Feedback for µC of the state of the motor connection of pin SH2 referred to voltage at VDHP. Connect to PFB 2 port to µC. If not used keep pin open.
55	PFB1	*Phase Voltage Feedback 1* Digital output pin referred to VCC supply voltage. Feedback for µC of the state of the motor connection of pin SH1 referred to voltage at VDHP. Connect to PFB 1 port to µC. If not used keep pin open.
56	ISN2	*Input Shunt Negative of CSA 2* Negative input of current sense amplifier 2 for shunt signal amplification. An external input filter is recommended. If current sense amplifier 2 is not used the pin shall be connected to GND and deactivate CSA 2 at configuration mode.
57	ISP2	*Input Shunt Positive of CSA 2* Positive input of current sense amplifier 2 for shunt signal amplification. An external input filter is recommended. If current sense amplifier 2 is not used the pin shall be connected to GND and deactivate CSA 2 at configuration mode.
58	VO2	*Voltage Output of CSA 2* Analog output of current sense amplifier 2 for shunt signal amplification referred to 5 V. Connect to analog-to-digital converter.
59	VRO	*Voltage Reference Output* Output pin of reference voltage of current sense amplifier. The reference voltage indicates the zero motor current output voltage. Connect to analog-to-digital converter.
60	VO1	*Voltage Output of CSA 1* Analog output of current sense amplifier 1 for shunt signal amplification referred to 5 V. Connect to analog-to-digital converter.
61	ISP1	*Input Shunt Positive of CSA 1* Positive input of current sense amplifier 1 for shunt signal amplification. An external input filter is recommended. If current sense amplifier 1 is not used the pin shall be connected to GND and deactivate CSA 1 at configuration mode.
62	ISN1	*Input Shunt Negative of CSA 1* Negative input of current sense amplifier 1 for shunt signal amplification. An external input filter is recommended. If current sense amplifier 1 is not used the pin shall be connected to GND and deactivate CSA 1 at configuration mode.
63	AGND	*Analog Ground* GND pin of current sense amplifier. Connect directly (low ohmic and low inductive) to GND.
64	ENA	*Enable* Digital input pin to turn all FETs off referred to VCC supply voltage. Functional independent to $\overline{\text{SOFF}}$ pin. Reset of latched error conditions.
Cooling Tab	GND	*Cooling Tab* To be connected to GND

2 General Failure Behavior Timing Diagrams

This chapter shows the difference between the four programmable failure behaviors of the gate driver IC.

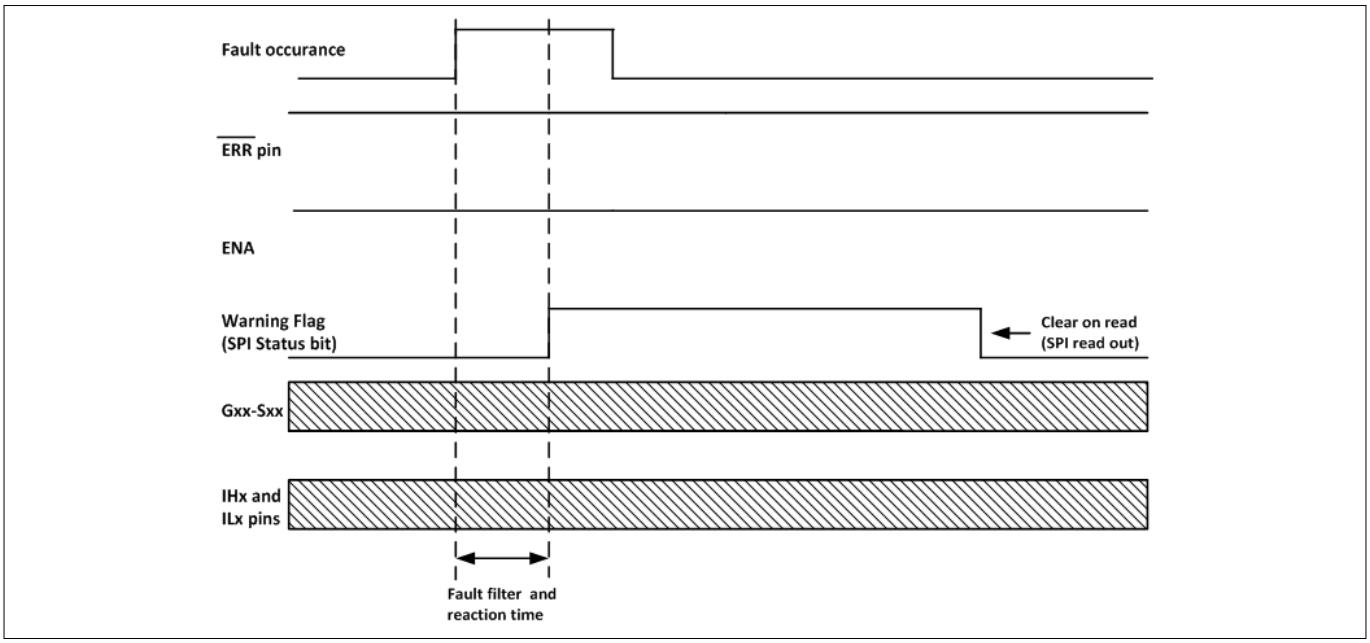


Figure 1 Timing Diagram Warning - Transient Fault Occurrence

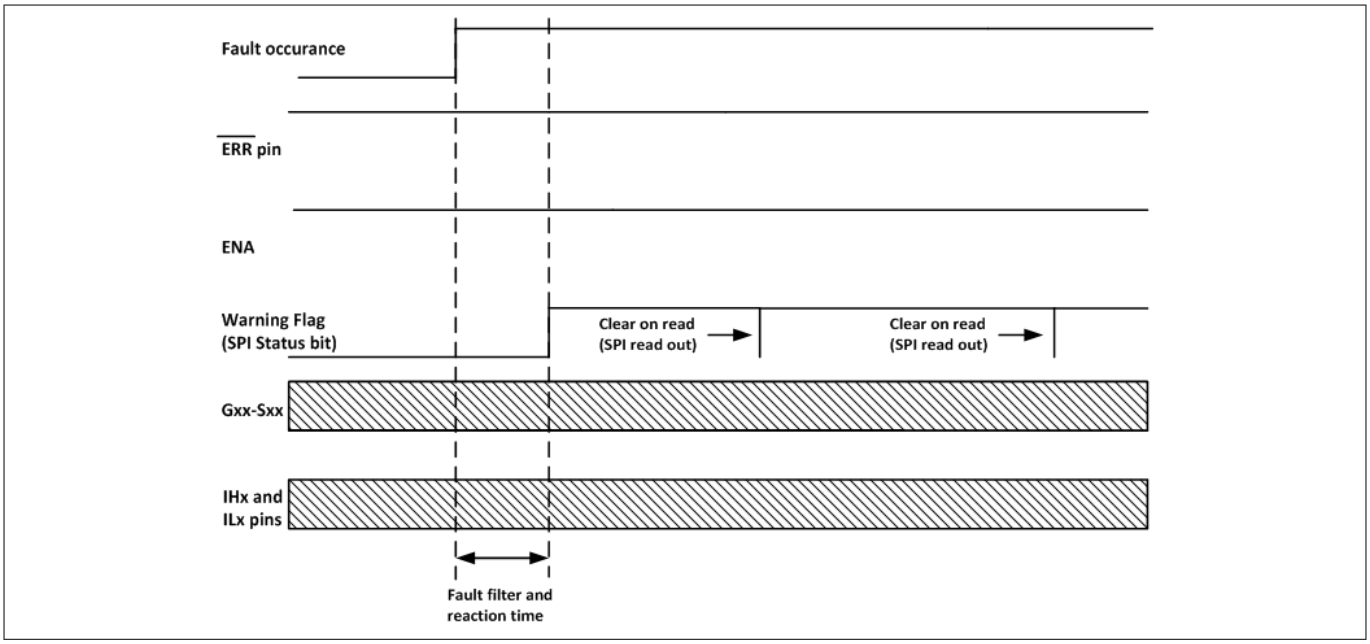


Figure 2 Timing Diagram Warning - Permanent Fault Occurrence

General Failure Behavior Timing Diagrams

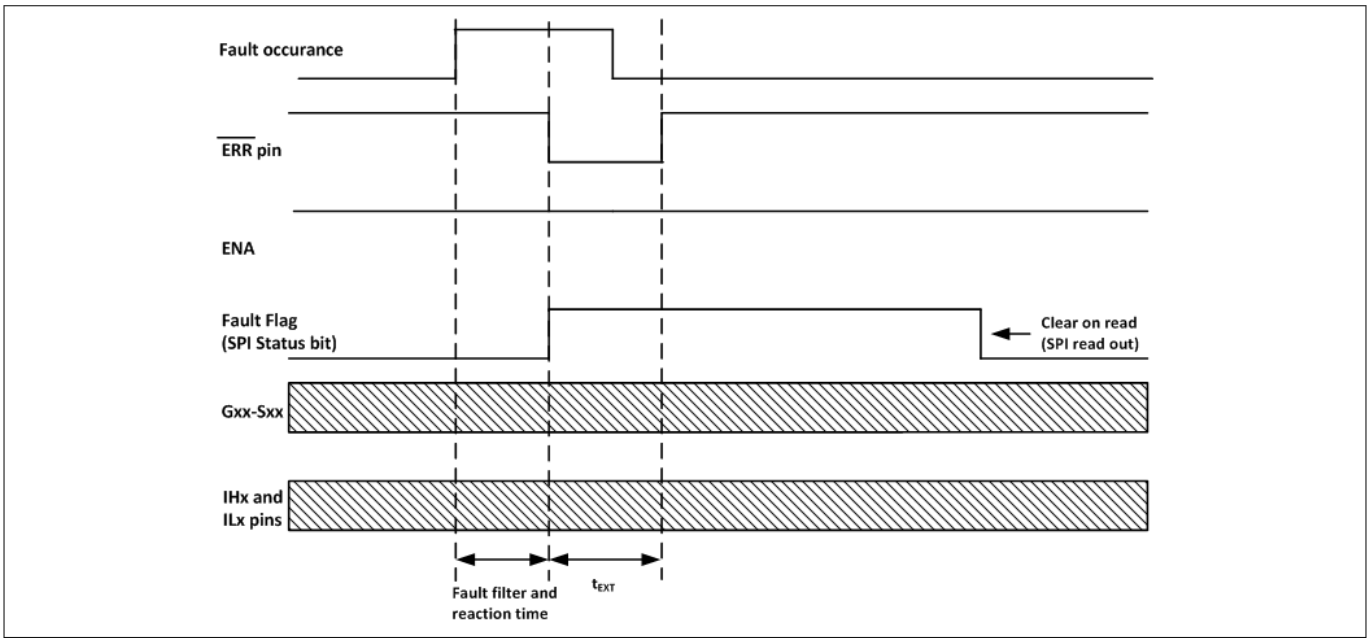


Figure 3 Timing Diagram Error - Transient Fault Occurrence

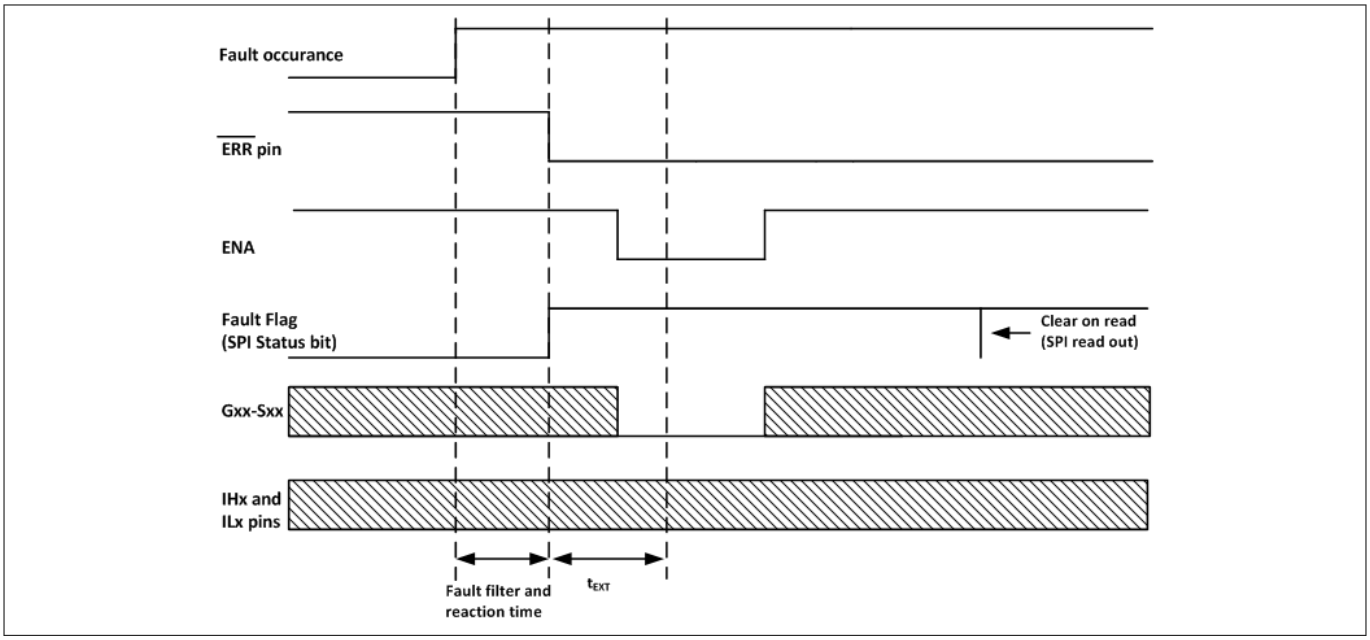


Figure 4 Timing Diagram Error - Permanent Fault Occurrence

General Failure Behavior Timing Diagrams

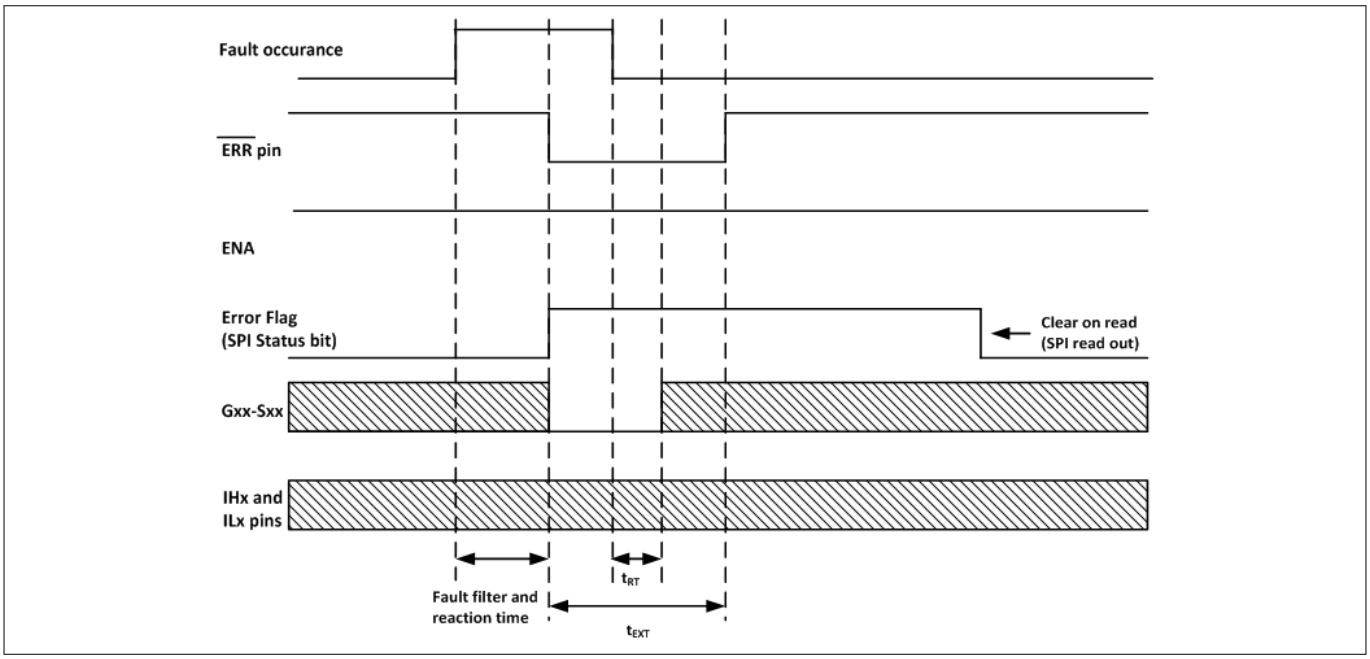


Figure 5 Timing Diagram Auto Restart Error - Transient Fault Occurrence

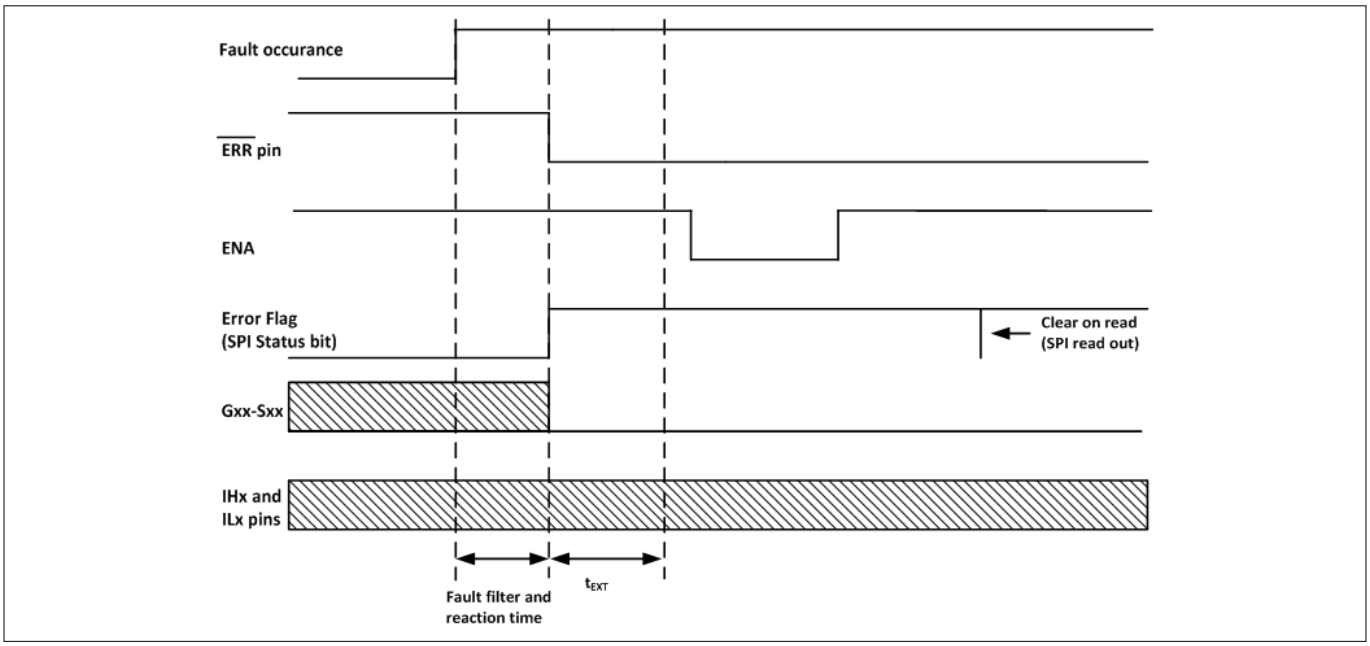


Figure 6 Timing Diagram Auto Restart Error - Permanent Fault Occurrence

General Failure Behavior Timing Diagrams

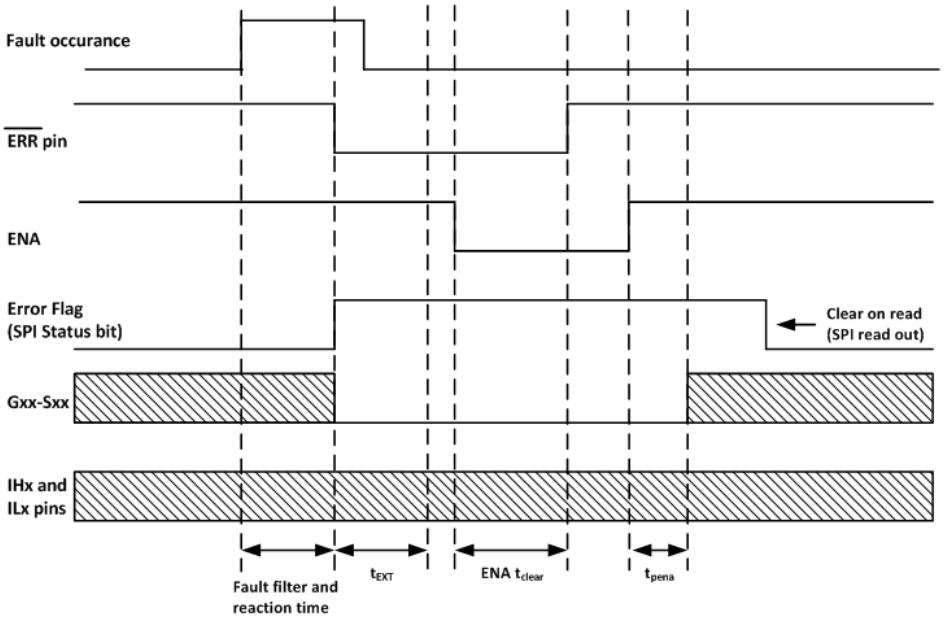
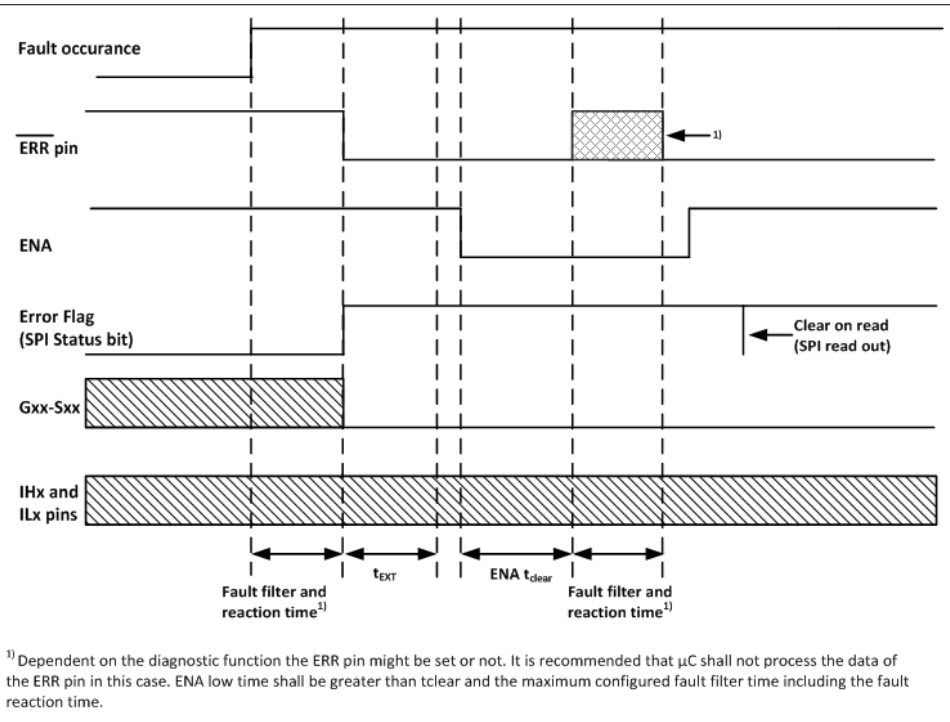


Figure 7 Timing Diagram Latched Error - Transient Fault Occurrence



1) Dependent on the diagnostic function the ERR pin might be set or not. It is recommended that µC shall not process the data of the ERR pin in this case. ENA low time shall be greater than tclear and the maximum configured fault filter time including the fault reaction time.

Figure 8 Timing Diagram Latched Error - Permanent Fault Occurrence

General Failure Behavior Timing Diagrams

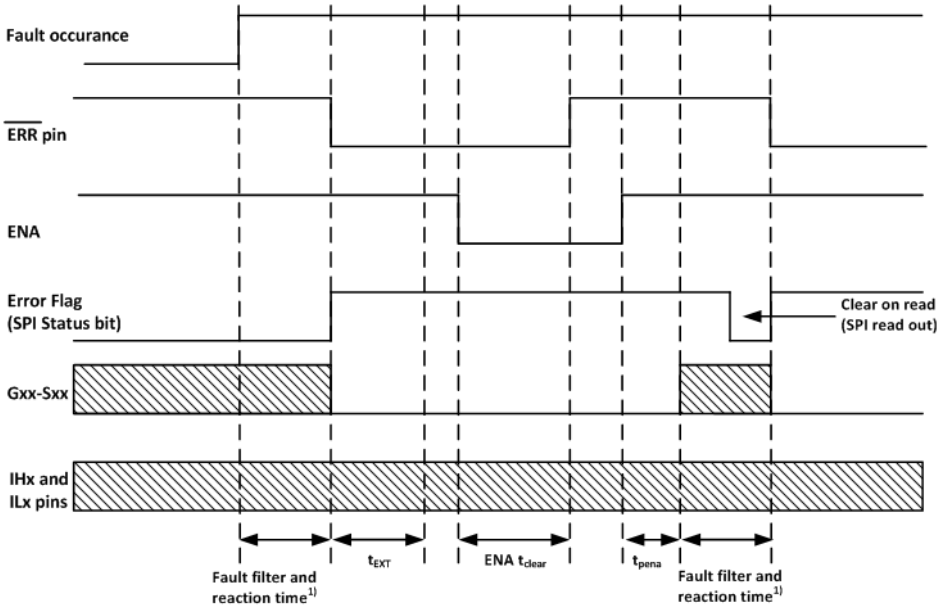


Figure 9 Timing Diagram Latched Error for Diagnosis SCD - Permanent Fault Occurrence

3 Phase Cut Off Activation

This chapter provides additional information to the chapter in TLE9183 Data Sheet Phase Cut Off Activation.

3.1 Phase Cut Off Programming

Table 1 Failure Detection for APC Activation

Bit Name	Bit Value	Detection	Bit Value	Detection
fm_act_apct	00	No APC Pin Triggering SPI status flag: Special event set if triggered by WWD Register Ser (0x42): bit apc_act set if triggered by WWD	10	Pin APC triggered by Window Watchdog or OV VCC SPI status flag: Special event set only if triggered by WWD Register Ser (0x42): bit apc_act set only if triggered by WWD SPI status flag: warning or Error set only if triggered by OV VCC[1)] Register Err_e (0x45): bit err_ov_vcc set if triggered by OV VCC
	01 (default)	Pin APC triggered by Window Watchdog SPI status flag: Special event set Register Ser (0x42): bit apc_act set	11	Pin APC triggered by Window Watchdog or UV VCC or OV VCC SPI status flag: Special event set only if triggered by WWD Register Ser (0x42): bit apc_act set only if triggered by WWD[1)] SPI status flag: warning or Error set only if triggered by UV VCC or OV VCC Register Err_e (0x45): bit err_uv_vcc or err_ov_vcc set if triggered by UV VCC or OV VCC

Table 2 Delay of Phase Cut Off Activation

Bit Name	Bit Value	Delay	Bit Value	Period
apc_tact	000	0 ms	100	30 ms
	001	5 ms	101	50 ms
	010	10 ms	110	75 ms
	011 (default)	20 ms	111	100 ms

1 Which SPI status flag is set depends on configured failure behavior. Statement is valid also for pin $\overline{\text{ERR}}$ if it is set or not.

Table 3 Configuration of pin APC functionality

Bit Name	Bit Value	APC activated	Normal Mode	Bit Value	APC activated	Normal Mode
apc_conf	00	Low	High	10 (default)	Stuck	Oscillating
	01	High	Low	11	Reserved	Reserved

3.2 Electrical Parameter Activation Phase Cut Off

Table 4 Electrical Characteristics - Phase Cut Off Activation

V_S = 5.5 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay of APC pin activation[2)]	t_{dAPC}	5	–	100	ms	8 steps programmable	P_13.2.1
APC oscillating frequency	f_{APC}	–	20	–	kHz	apc_conf = ’10’	P_13.2.2
APC oscillating frequency Duty Cycle	$D.C._{APC}$	–	50	–	%	apc_conf = ’10’	P_13.2.3

2 Internal clock frequency accuracy has to be added to the specified values, please see Electrical Characteristics Clock in Data Sheet

4 Self Test Mode

Self-test functionality has been integrated for certain diagnosis features. Of course during self-diagnosis these supervisions are not functional. Self-test mode is not allowed to be entered accidentally. Therefore a self-test mode entry finite state machine is designed. The FSM consists of 3 states, only the 3rd one enables the self-test mode. The entry sequence shall not be interrupted by any other SPI frame, otherwise the sequence has to be sent again. The different self-tests have to be initiated sequentially. The self-tests themselves have different priorities. So if two self-tests are selected at the same time only the self-test with higher priority will be performed. The µC has to reset the bit self-test mode enabled and set the bit self-test mode disabled to leave the self-test mode. The different self-test functions and the priority is listed in the latest Data Sheet of TLE9183 in Diagnostic Test Functions.

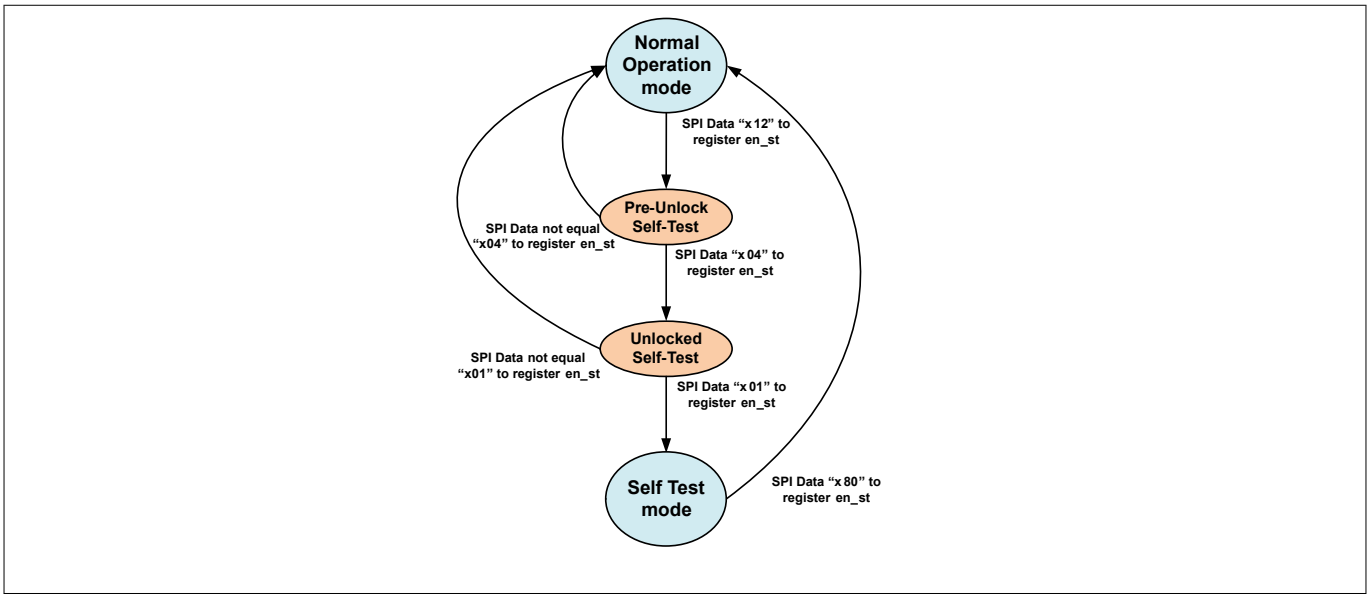


Figure 10 Self-test Mode Entry and Exit Sequence

For detailed explanation and description of the available self tests please refer to the safety manual of TLE9183QK.

4.1 Self-test Function for VCC

To ensure the monitoring works properly a VCC self-test is available. If activated a fixed voltage level will be applied at the input of the supervision circuit. The applied voltage level is below the VCC undervoltage detection level so undervoltage VCC will occur. The self-test bit has to be cleared to exit the undervoltage VCC self-test.

4.2 Self-test Function for SCD

The SCD function can be tested. If self-test SCD high-side is activated a fixed voltage level will be applied at the input of the SCD supervision circuit. The voltage level is higher as the maximum adjustable short circuit detection level so short circuit has to be detected. If the fault behavior is configured as error, auto restart or latched error and then the self-test SCD high-side is activated and either $\overline{\text{ERR}}$ pin is not set nor the dedicated error bit is set, the short circuit detection won't operate as specified. The self-test SCD low-side checks the negative input range of the SCD-comparator. The result of the comparator is written into the registers. In case both SCD self-tests have been performed and the value of the read out registers is 0x80 at self-test SCD LS and 0x7F at the self-test SCD HS the input comparator operates as specified. The self-test bit has to be cleared to exit the short circuit detection self-test. It is recommended to keep pin ENA high for the entire self test sequence.

Self Test Mode

The fault reaction of the short circuit detection can be tested in normal operation mode. If a negative threshold of 0xEE is applied and the affected external FET is turned on, the device will detect short circuit after the blank- and filter time has expired. During this test no current shall flow from source to drain of the external affected FET.

5 Register Description

This chapter includes the detailed information on SPI data flow and how received and transmitted data frames look like. All registers are listed in ***Register Specification***.

5.1 SPI Data Flow

Registers can be accessed via read or write command. The response to the current SPI command will be send with next SPI command. If the information of the current SPI command is required immediately, the µC shall send the no operation command directly after the initial request.

5.2 SPI Frame Format

A SPI frame contains 24 bit. For all fields, address and data, the most significant is received and sent first. The first received bit C determines a read or write command. C set to high indicates a write command, C set to low a read access.

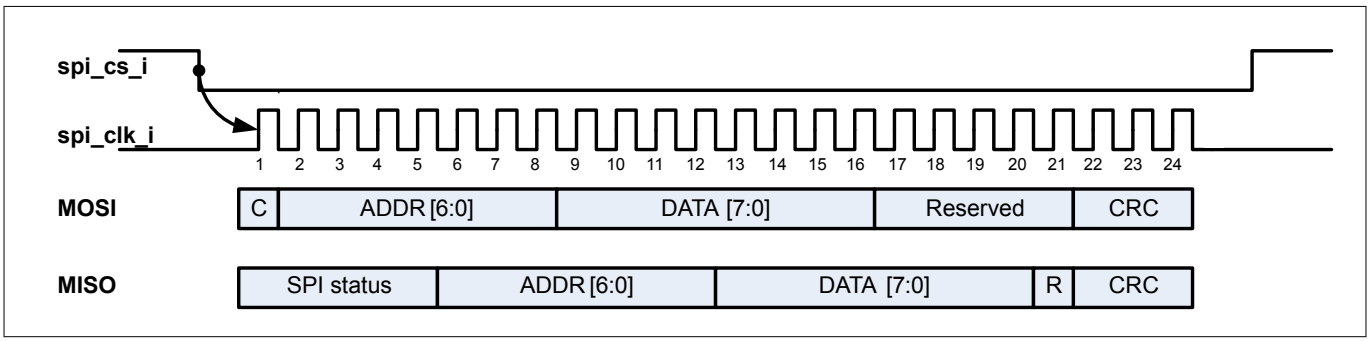


Figure 11 SPI Frame Format

5.2.1 SPI Status Flags

The SPI status flags are transmitted in any response. The SPI status flags contain the following information.

Table 5 SPI Status Flags

Bit position	Flag	Description
1	Error	ERR, ARE and LE indication via SPI
2	Warning	Warning indication via SPI
3	Config Valid	Configuration registers valid
4	SPI-Error	Please see ***Table 6***
5	Special Event	Please see ***Table 7***

SPI Status Flag Error, Warning and Special Event

The SPI status flags Error, Warning or Special Event in a transmitted frame (MISO) indicate the status of the device according to the current register value. If the fault is not present anymore and the indicated fault is cleared by a read command (MOSI) of a register 0x41 to 0x4D (except register 0x4A) the fault is not visible in the SPI status flags. In this case the error information can only be seen once in the detailed error bit of the transmitted error register (transmitted data of error-register 0x41 to 0x4D (except register 0x4A)). It can only be detected by the SPI status flags of the previous transmitted SPI frame (MISO), if the fault was already present at that time. The bits 2, 5 and 6 of the register 0x4A, for details see ***Table 6*** set the SPI status flags only once and it is cleared after the next valid SPI frame automatically. For details please contact Infineon.

SPI Status Flag Config Valid

The behavior of the SPI status flag Config Valid is described in Chapter "Configuration Signature Invalid" in the Data Sheet.

SPI Status SPI-Error

The behavior of the SPI status flaf SPI-Error is described in ***Chapter 5.3***.

5.3 SPI Supervision Overview

The SPI communication and the access to registers is supervised for various failures. They are all summarized in the register 0x4A SPI Communication and Configuration Errors bit 0, 1, 3 and 4. These bits triggers the SPI status flag SPI-Error. The SPI status flag SPI-Error is set and transmitted with the next data communication. It is cleared with the next valid transfer so it can only be seen once. The bits 0, 1, 3 and 4 are not cleared. These bits are cleared after read.

5.3.1 Overview of SPI Communication and Configuration Errors

The error bits of the register SPI communication and configuration errors triggers the SPI status flags as shown in ***Table 6***.

Table 6 Overview of SPI Communication and Configuration Error

Bit #	Bit Name	Error Condition	SPI Status Flag
0	err_spi_frame	SPI Frame Error	SPI-Error
1	err_spi_to	SPI Time-out Error	SPI-Error
2	err_spi_wd	SPI Watchdog Time-out	Error
3	err_spi_crc	CRC Error (incoming data)	SPI-Error
4	spi_add_invalid	Invalid Address Access	SPI-Error
5	conf_to	Configuration Time-out	Error
6	conf_sig_invalid	Sent Configuration Signature Byte Invalid	Error
7	Reserved	Reserved	Reserved

5.3.2 Overview of Special Event Register

Following table shows which bits will set the special event flag of the SPI status flags.

Table 7 Overview of Special Event Register

Bit #	Bit Name	Description
0	rom	Reduced Operation Mode Occurred
1	limp_on	Limp Home Active
2	Reserved	Reserved
3	apc_act	Phase Cut off Activation[3)]

3 For details please refer to ***Table 1***

Table 7 Overview of Special Event Register (continued)

Bit #	Bit Name	Description
4	GTM	Global Test Mode active (not for customer usage, for information only).
5	crtl_reg_invalid	Error Correction of Control Register Failed
6	lfw	Latent Fault Warning
7	err_ot_w	Overtemperature Detection

5.3.3 Reserved Registers, Bits and Values

Following table describes the recommended software handling regarding to reserved area.

Table 8 Overview of Software Handling of Reserved Areas

Reserved Area	Software Handling
Registers	Read and write access to register addresses which are not specified shall not be performed
Bits in register	Bit values of reserved bits shall be left unchanged
Bit in SPI frame	'0' shall be written into the reserved bits of the SPI frame, shown in ***Figure 11***
Values	Writing reserved values, e.g. set bit 1 and bit 0 to '1' shall not be performed

5.3.4 Overview of Register Types

This chapter gives an overview the different register types of the device.

Table 9 Access Type Abbreviations

Access Type	Description
r	Bits are readable (read)
rc	Bits are readable and value is cleared after read access (clear-on-read)
rw	Bits are read- and writeable (read-write)
rwc	Bits are readable and writeable, bits will be cleared automatically after initiated routine has been finished (read-write-clear)
rmw	Bits are readable, bits are writeable only in configuration mode (read-monostable-write)

Table 10 Register Type Overview

Register Type	Access Type	Address Range	Read Access	Write Access
Configuration	rmw	0x00H-0x1FH	Idle-, configuration -, configuration lock-, normal operation-, self test-, safe off- and error mode	Configuration mode
Control	rw & rwc	0x20H-0x34H	Idle-, configuration -, configuration lock-, normal	Idle-, configuration -, configuration lock-, normal

Table 10 Register Type Overview (continued)

Register Type	Access Type	Address Range	Read Access	Write Access
			operation-, self test-, safe off- and error mode	operation-, self test-, safe off- and error mode
Self Test	rw & rwc	0x35H-0x37H	Idle-, configuration -, configuration lock-, normal operation-, self test-, safe off- and error mode	Self-test mode
Read	r & rc	0x40H-0x67H	Idle-, configuration -, configuration lock-, normal operation-, self test-, safe off- and error mode	none

6 Register Specification

6.1 Registers Chapter

Table 11 Registers Address Space

Module	Base Address	End Address	Note
BusInterface	0_H	FF_H	Slave interface

Table 12 Register Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
Conf_Sig	Configuration Signature	00_H	BA_H
Conf_Gen_1	General Configuration 1	01_H	80_H
Conf_Gen_2	General Configuration 2	02_H	03_H
Conf_Gen_3	General Configuration 3	03_H	$1C_H$
Conf_wwd	Window Watchdog	04_H	56_H
Tl_vs	Vs Over- and Undervoltage Thresholds	05_H	07_H
Tl_vdh	VDHP Over- and Undervoltage Thresholds	06_H	$A0_H$
Tl_cbvcc	CB Under- and VCC Under- and Overvoltage Thresholds	07_H	95_H
Fm_1	Charge Pump/High-side Buffer Failure Modes	08_H	30_H
Fm_2	Miscellaneous Failure Modes	09_H	70_H
Fm_3	Vs & VDHP & VCC Undervoltage Failure Modes	$0A_H$	10_H
Fm_4	Vs & VDHP & VCC Overvoltage Failure Modes	$0B_H$	20_H
Fm_5	Short Circuit Detection & Signal Path Supervision Failure Modes	$0C_H$	60_H
Dt_hs	Dead Time High-side	$0D_H$	$0E_H$
Dt_ls	Dead Time Low-side	$0E_H$	$0E_H$
Ft_1	Undervoltage Filter Times	$0F_H$	85_H
Ft_2	Overvoltage and VCC Filter Times	10_H	50_H
Ft_3	Overtemperature & Short Circuit Detection Filter Times	11_H	$0E_H$
Ft_4	Overcurrent Filter Time	12_H	02_H
Fm_6	Overcurrent Failure Modes	13_H	00_H
Op_gain_1	Current Sense Amplifier 1&2 - Gain 1	20_H	33_H
Op_gain_2	Current Sense Amplifier 1&2 - Gain 2	21_H	55_H
Op_gain_3	Current Sense Amplifier 3 - Gain 1&2	22_H	53_H
Op_0cl	Current Sense Amplifier Zero Current Offset	23_H	$5F_H$
op_con	Current Sense Amplifier Configuration	24_H	07_H

Table 12 Register Overview (continued)

Register Short Name	Register Long Name	Offset Address	Reset Value
Sc_ls_1	Short Circuit Detection Threshold Low-side 1	25_H	$1A_H$
Sc_ls_2	Short Circuit Detection Threshold Low-side 2	26_H	$1A_H$
Sc_ls_3	Short Circuit Detection Threshold Low-side 3	27_H	$1A_H$
Sc_hs_1	Short Circuit Detection Threshold High-side 1	28_H	$1A_H$
Sc_hs_2	Short Circuit Detection Threshold High-side 2	29_H	$1A_H$
Sc_hs_3	Short Circuit Detection Threshold High-side 3	$2A_H$	$1A_H$
Li_ctr	Limp Home Activation and Half Bridge Deactivation	$2B_H$	$E8_H$
Misc_ctr	Shift Phase Voltage Feedback and CSA Gain	$2C_H$	00_H
art_tlp	Passive Rectification Threshold	$2D_H$	$F8_H$
art_tla	Active Rectification Threshold	$2E_H$	06_H
art_fi	Rectification Filter Time	$2F_H$	53_H
art_acc	Rectification Accuracy	30_H	21_H
art_entry	Rectification Mode entry	31_H	80_H
nop	No Operation	32_H	00_H
Drev_mark	Reverse Diode Measurement	33_H	00_H
Ds_mark	Drain Source Measurement	34_H	00_H
Sel_st_1	Self Test Selection 1	35_H	00_H
Sel_st_2	Self Test Selection 2	36_H	00_H
En_st	Self Test Mode Entry	37_H	80_H
Om_over	Operation Mode Overview	40_H	00_H
Err_over	Error Overview	41_H	00_H
Ser	Special Event Register	42_H	00_H
Err_i_1	Internal Errors 1	43_H	00_H
Err_i_2	Internal Errors 2	44_H	00_H
Err_e	External Errors	45_H	00_H
Err_sd	Shutdown Errors	46_H	00_H
Err_scd	Short Circuit Errors	47_H	00_H
Err_indiag	Input Pattern Violations	48_H	00_H
Err_osf	Output Stage Feedback Errors	49_H	00_H
Err_spiconf	SPI Communication and Configuration Errors	$4A_H$	00_H
Err_op_12	Current Sense Amplifiers 1 & 2 Errors	$4B_H$	00_H
Err_op_3	Current Sense Amplifier 3	$4C_H$	00_H
Err_outp	Digital Output Pin Errors	$4D_H$	00_H

Table 12 Register Overview (continued)

Register Short Name	Register Long Name	Offset Address	Reset Value
dsm_ls1	Low-side 1 Drain Source Measurement	$4E_H$	00_H
dsm_ls2	Low-side 2 Drain Source Measurement	$4F_H$	00_H
dsm_ls3	Low-side 3 Drain Source Measurement	50_H	00_H
dsm_hs1	High-side 1 Drain Source Measurement	51_H	00_H
dsm_hs2	High-side 2 Drain Source Measurement	52_H	00_H
dsm_hs3	High-side 3 Drain Source Measurement	53_H	00_H
Rdm_ls1	Low-side 1 Reverse Diode Measurement	54_H	00_H
Rdm_ls2	Low-side 2 Reverse Diode Measurement	55_H	00_H
Rdm_ls3	Low-side 3 Reverse Diode Measurement	56_H	00_H
Rdm_hs1	High-side 1 Reverse Diode Measurement	57_H	00_H
Rdm_hs2	High-side 2 Reverse Diode Measurement	58_H	00_H
Rdm_hs3	High-side 3 Reverse Diode Measurement	59_H	00_H
temp_ls1	Low-side 1 Output Stage Temperature	$5A_H$	00_H
temp_ls2	Low-side 2 Output Stage Temperature	$5B_H$	00_H
temp_ls3	Low-side 3 Output Stage Temperature	$5C_H$	00_H
temp_hs1	High-side 1 Output Stage Temperature	$5D_H$	00_H
temp_hs2	High-side 2 Output Stage Temperature	$5E_H$	00_H
temp_hs3	High-side 3 Output Stage Temperature	$5F_H$	00_H
wwlc	Window Watchdog Loop Counter	60_H	00_H
res_cc1	Watchdog Clock Counter 1	61_H	00_H
res_cc2	Watchdog Clock Counter 2	62_H	00_H
res_cc3	Watchdog Clock Counter 3	63_H	00_H
res_vcc	VCC Measurement Result	64_H	00_H
res_cb	CB Measurement Result	65_H	00_H
res_vs	Vs Measurement Result	66_H	00_H
res_vdh	VDHP Measurement Result	67_H	00_H

Registers Access

The registers are addressed wordwise.

6.1.1 Configuration registers

6.1.1.1 Configuration Signature

Conf_Sig Address: 00_H

Configuration Signature Reset value: BA_H

7	6	5	4	3	2	1	0
CRC							
rmw							

Field	Bits	Type	Description
CRC	7:0	rmw	**CRC8 Signature Byte** 10111010_B , CRC8 for default configuration register values

6.1.1.2 General Configuration 1

Conf_Gen_1 Address: 01_H

General Configuration 1 Reset value: 80_H

7	6	5	4	3	2	1	0
tl_ot_w			**in_diag_act**	**spi_wwd_act**	**limp_act**	**vcc_sup_off**	**vcc_select**
rmw			rmw	rmw	rmw	rmw	rmw

Field	Bits	Type	Description
tl_ot_w	7:5	rmw	**Overtemperature Detection Threshold** 111_B , 125°C 110_B , 130°C 101_B , 135°C 100_B , 140°C (default) 011_B , 145°C 010_B , 150°C 001_B , 155°C 000_B , 160°C
in_diag_act	4	rmw	**Input Pattern Supervision** 1_B , Enabled 0_B , Disabled (default)
spi_wwd_act	3	rmw	**SPI Window Watchdog** 1_B , Enabled 0_B , Disabled (default)
limp_act	2	rmw	**Limp Home Mode Activation** 1_B , Enabled 0_B , Disabled (default)
vcc_sup_off	1	rmw	**VCC Supervision** 1_B , Disabled 0_B , Enabled (default)
vcc_select	0	rmw	**VCC Monitoring Threshold** 1_B , 5V selected as VCC supply voltage 0_B , 3.3V selected as VCC supply voltage (default)

6.1.1.3 General Configuration 2

Conf_Gen_2 Address: 02_H

General Configuration 2 Reset value: 03_H

7	6	5	4	3	2	1	0
tl_oc_op	**dis_ov_bh**	**dis_ov_ld_vdh**	**dis_sd_vdh**	**en_vdh3**	**en_op3**	**en_op2**	**en_op1**
rmw	rmw	rmw	rmw	rmw	rmw	rmw	rmw

Field	Bits	Type	Description
tl_oc_op	7	rmw	**Threshold Level Overcurrent Detection Current Sense Amplifiers** 1_B , 3.3V Overcurrent Detection Threshold 0_B , 5V Overcurrent Detection Threshold (default)
dis_ov_bh	6	rmw	**Disable Overvoltage Detection of High-side Buffer Capacitors** 1_B , OV BSx disabled 0_B , OV BSx enabled (default)
dis_ov_ld_vdh	5	rmw	**Disable Load Dump Overvoltage Detection at pin VDHP** 1_B , OV LD disabled 0_B , OV LD enabled (default)
dis_sd_vdh	4	rmw	**Disable Shutdown at VDHP** 1_B , OV SD VDHP disabled 0_B , OV SD VDHP enabled (default)
en_vdh3	3	rmw	**Enable 3 VDHx sense pins** 1_B , 3 VDH sense pins and 1 VDHP power pin enabled 0_B , 1 VDHP pin selected (default)
en_op3	2	rmw	**Enable Current Sense Amplifier 3** 1_B , Current Sense Amplifier 3 enabled 0_B , Current Sense Amplifier 3 deactivated (default)
en_op2	1	rmw	**Enable Current Sense Amplifier 2** 1_B , Current Sense Amplifier 2 enabled (default) 0_B , Current Sense Amplifier 2 deactivated
en_op1	0	rmw	**Enable Current Sense Amplifier 1 and Reference Output Buffer** 1_B , Current Sense Amplifier 1 and Reference Output Buffer enabled (default) 0_B , Current Sense Amplifier 1 and Reference Output Buffer deactivated

6.1.1.4 General Configuration 3

Conf_Gen_3 Address: 03_H

General Configuration 3 Reset value: $1C_H$

7	6	5	4	3	2	1	0
Res	**en_ART**	**apc_tact**			**apc_conf**		**art_scd**
none	rmw	rmw			rmw		rmw

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
en_ART	6	rmw	**Enable ART pin** 1_B , ART pin enabled; APC disabled 0_B , APC pin enabled; ART disabled (default)
apc_tact	5:3	rmw	**Timing Activation of Active Phase Cut Off (APC)** 111_B , 100 ms 110_B , 75 ms 101_B , 50 ms 100_B , 30 ms 011_B , 20 ms (default) 010_B , 10 ms 001_B , 5 ms 000_B , 0 ms
apc_conf	2:1	rmw	**Active Phase Cut Off (APC) Output Signal Configuration** 11_B , Reserved 10_B , Active stuck - oscillating in normal mode (default) 01_B , Active high 00_B , Active low
art_scd	0	rmw	**Failure Behavior of Short Circuit Detection in ART Mode** 1_B , ARE - Short Circuit Detection and output stages deactivated with auto restart 0_B , ARE - Short Circuit Detection only (default)

6.1.1.5 Window Watchdog

Conf_wwd Address: 04_H

Window Watchdog Reset value: 56_H

7	6	5	4	3	2	1	0
wwd_count			**wwd_ratio**			**wwd_tp**	
rmw			rmw			rmw	

Field	Bits	Type	Description
wwd_count	7:5	rmw	**Loop Counter of Window Watchdog (increment 2; decrement 1)** 111_B , 16 110_B , 14 101_B , 12 100_B , 10 011_B , 8 010_B , 6 (default) 001_B , 4 000_B , 2
wwd_ratio	4:2	rmw	**Ratio between Locked and Evaluation Window** 111_B , 95% 110_B , 92% 101_B , 90% (default) 100_B , 80% 011_B , 75% 010_B , 70% 001_B , 60% 000_B , 50%
wwd_tp	1:0	rmw	**Period of Window Watchdog** 11_B , 10 ms 10_B , 5 ms (default) 01_B , 2 ms 00_B , 1 ms

6.1.1.6 Vs Over- and Undervoltage Thresholds(User Manual version)

Tl_vs Address: 05_H

Vs Over- and Undervoltage Thresholds Reset value: 07_H

7	6	5	4	3	2	1	0
tl_ov_vs				**tl_uv_vs**			
rmw				rmw			

Field	Bits	Type	Description
tl_ov_vs	7:4	rmw	**Vs Overvoltage Threshold** 1111_B , reserved V 1110_B , reserved V 1101_B , reserved V 1100_B , reserved V 1011_B , reserved V 1010_B , reserved V 1001_B , reserved V 1000_B , reserved V 0111_B , 39.95 V 0110_B , 35.98 V 0101_B , 34.15 V 0100_B , 32.02 V 0011_B , 28.05 V 0010_B , 24.09 V 0001_B , 20.13 V 0000_B , 18.00 V (default)
tl_uv_vs	3:0	rmw	**Vs Undervoltage Threshold** 1111_B , 9.45 V 1110_B , 9.15 V 1101_B , 8.84 V 1100_B , 8.54 V 1011_B , 8.23 V 1010_B , 7.93 V 1001_B , 7.62 V 1000_B , 7.32 V 0111_B , 7.01 V (default) 0110_B , 6.71 V 0101_B , 6.40 V 0100_B , 6.10 V 0011_B , 5.79 V 0010_B , 5.49 V 0001_B , 5.18 V 0000_B , 4.88 V

6.1.1.7 VDHP Over- and Undervoltage Thresholds(User Manual version)

Tl_vdh Address: 06_H

VDHP Over- and Undervoltage Thresholds Reset value: $A0_H$

7	6	5	4	3	2	1	0
tl_ov_vdh				**tl_uv_vdh**			
rmw				rmw			

Field	Bits	Type	Description
tl_ov_vdh	7:4	rmw	**VDHP Overvoltage Threshold** 1111_B , reserved V 1110_B , reserved V 1101_B , reserved V 1100_B , reserved V 1011_B , reserved V 1010_B , 56.11 V (default) 1001_B , reserved V 1000_B , reserved V 0111_B , 48.18 V 0110_B , 39.95 V 0101_B , 35.98 V 0100_B , 32.02 V 0011_B , 28.05 V 0010_B , 24.09 V 0001_B , 20.13 V 0000_B , 18.00 V
tl_uv_vdh	3:0	rmw	**VDHP Undervoltage Threshold** 1111_B , reserved V 1110_B , reserved V 1101_B , reserved V 1100_B , reserved V 1011_B , reserved V 1010_B , reserved V 1001_B , reserved V 1000_B , reserved V 0111_B , 10.06 V 0110_B , 9.15 V 0101_B , 7.93 V 0100_B , 7.01 V 0011_B , 6.10 V 0010_B , 5.49 V 0001_B , 4.88 V 0000_B , 3.96 V (default)

6.1.1.8 CB Under- and VCC Under- and Overvoltage Thresholds

Tl_cbvcc Address: 07_H

CB Under- and VCC Under- and Overvoltage Thresholds Reset value: 95_H

7	6	5	4	3	2	1	0
tl_uv_cb				**tl_ov_vcc**		**tl_uv_vcc**	
rmw				rmw		rmw	

Field	Bits	Type	Description
tl_uv_cb	7:4	rmw	**CB Undervoltage Threshold** 1111_B , 10.44 V 1110_B , 10.22 V 1101_B , 9.99 V 1100_B , 9.76 V 1011_B , 9.53 V 1010_B , 9.30 V 1001_B , 9.07 V (default) 1000_B , 8.84 V 0111_B , 8.61 V 0110_B , 8.39 V 0101_B , 8.16 V 0100_B , 7.93 V 0011_B , 7.70 V 0010_B , 7.47 V 0001_B , 7.24 V 0000_B , 7.01 V
tl_ov_vcc	3:2	rmw	**VCC Overvoltage Threshold** 11_B , Reserved 10_B , 10% of configured VCC supply voltage 01_B , 4% of configured VCC supply voltage 00_B , Reserved
tl_uv_vcc	1:0	rmw	**VCC Undervoltage Threshold** 11_B , Reserved 10_B , 10% of configured VCC supply voltage 01_B , 4% of configured VCC supply voltage 00_B , Reserved

6.1.1.9 Charge Pump/High-side Buffer Failure Modes

Fm_1 Address: 08_H

Charge Pump/High-side Buffer Failure Modes Reset value: 30_H

7	6	5	4	3	2	1	0
fm_uv_cb		**Res**	**fm_cp2_off**	**Res**		**fm_uv_bs**	
rmw		none	rmw	none		rmw	

Field	Bits	Type	Description
fm_uv_cb	7:6	rmw	**CB Undervoltage Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)
Res	5	none	**Reserved** 1_B , default value. do not change.
fm_cp2_off	4	rmw	**Overload Charge Pump 2 Failure Behavior** 1_B , Shutdown of output stages (default) 0_B , No shutdown of output stages
Res	3:2	none	**Reserved** 00_B , default value. do not change.
fm_uv_bs	1:0	rmw	**Undervoltage High-side Buffer Capacitor Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)

6.1.1.10 Miscellaneous Failure Modes

Fm_2 Address: 09_H

Miscellaneous Failure Modes Reset value: 70_H

7	6	5	4	3	2	1	0
fm_act_apc		**fm_spi_wwd**		**Res**		**fm_ot_w**	
rmw		rmw		none		rmw	

Field	Bits	Type	Description
fm_act_apc	7:6	rmw	**APC activation** 11_B , Triggered by VCC out of range and SPI Window Watchdog Time-out 10_B , Triggered by VCC Overvoltage and SPI Window Watchdog Time-out 01_B , Triggered by SPI Window Watchdog Time-out (default) 00_B , APC not triggered
fm_spi_wwd	5:4	rmw	**SPI Window Watchdog Time-out Failure Behavior** 11_B , LE - Latched Error (default) 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning
Res	3:2	none	**Reserved** 00_B , default value. do not change.
fm_ot_w	1:0	rmw	**Overtemperature Detection Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)

6.1.1.11 Vs & VDHP & VCC Undervoltage Failure Modes

Fm_3 Address: $0A_H$

Vs & VDHP & VCC Undervoltage Failure Modes Reset value: 10_H

7	6	5	4	3	2	1	0
Res		**fm_uv_vs**		**fm_uv_vdh**		**fm_uv_vcc**	
none		rmw		rmw		rmw	

Field	Bits	Type	Description
Res	7:6	none	**Reserved** 00_B , default value. do not change.
fm_uv_vs	5:4	rmw	**Vs Undervoltage Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error (default) 00_B , W - Warning
fm_uv_vdh	3:2	rmw	**VDHP Undervoltage Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)
fm_uv_vcc	1:0	rmw	**VCC Undervoltage Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)

6.1.1.12 Vs & VDHP & VCC Overvoltage Failure Modes

Fm_4 Address: $0B_H$

Vs & VDHP & VCC Overvoltage Failure Modes Reset value: 20_H

7	6	5	4	3	2	1	0
Res	**fm_ov_vs**		**fm_ov_vdh**			**fm_ov_vcc**	
none	rmw		rmw			rmw	

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
fm_ov_vs	6:5	rmw	**Vs Overvoltage Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error (default) 00_B , W - Warning
fm_ov_vdh	4:2	rmw	**VDHP Overvoltage Failure Behavior** 111_B , LE1 - Latched Error all HS FETs off only 110_B , ARE1 - Auto Restart Error all HS FETs off only 101_B , Reserved5 100_B , Reserved4 011_B , LE - Latched Error all FETs off 010_B , ARE - Auto Restart Error 001_B , ERR - Error 000_B , W - Warning (default)
fm_ov_vcc	1:0	rmw	**VCC Overvoltage Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)

6.1.1.13 Short Circuit Detection & Signal Path Supervision Failure Modes

Fm_5

Address: $0C_H$

Short Circuit Detection & Signal Path Supervision Failure Modes

Reset value: 60_H

7	6	5	4	3	2	1	0
fm_scd			**fm_outp_ol**	**fm_osfb**		**fm_in_diag**	
rmw			rmw	rmw		rmw	

Field	Bits	Type	Description
fm_scd	7:5	rmw	**Short Circuit Detection Failure Behavior** 111_B , LE2 - Latched Error, affected external FET off 110_B , LE1 - Latched Error, affected half bridge off 101_B , Reserved5 100_B , Reserved4 011_B , LE - Latched Error, all external FETs off (default) 010_B , ARE - Auto Restart Error 001_B , ERR - Error 000_B , W - Warning
fm_outp_ol	4	rmw	**Digital Output Pin Overload Failure Behavior** 1_B , Shutdown of output stages 0_B , No shutdown of output stages (default)
fm_osfb	3:2	rmw	**Output Stage Feedback Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)
fm_in_diag	1:0	rmw	**Input Pattern Supervision Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)

6.1.1.14 Dead Time High-side

Dt_hs Address: $0D_H$

Dead Time High-side Reset value: $0E_H$

7	6	5	4	3	2	1	0
dths							
rmw							

Field	Bits	Type	Description
dths	7:0	rmw	**Dead time for high-side output stages** [formula: value*35.7+107; unit: ns] 10100101_B , 6 µs - maximum dead time 00001110_B , 600 ns (default) 00000000_B , 107 ns - minimum dead time

6.1.1.15 Dead Time Low-side

Dt_ls Address: $0E_H$

Dead Time Low-side Reset value: $0E_H$

7	6	5	4	3	2	1	0
dtls							
rmw							

Field	Bits	Type	Description
dtls	7:0	rmw	**Dead time for low-side output stages** [formula: value*35.7+107; unit: ns] 10100101_B , 6 µs - maximum dead time 00001110_B , 600 ns (default) 00000000_B , 107 ns9 ns - minimum dead time

6.1.1.16 Undervoltage Filter Times

Ft_1

Undervoltage Filter Times

Address: $0F_H$

Reset value: 85_H

7	6	5	4	3	2	1	0
f_uv_bs		**f_uv_cb**		**f_uv_vdh**		**f_uv_vs**	
rmw		rmw		rmw		rmw	

Field	Bits	Type	Description
f_uv_bs	7:6	rmw	**High-side Buffer Capacitor Undervoltage Filter Time** 11_B , 10 µs 10_B , 5 µs (default) 01_B , 3 µs 00_B , 1 µs
f_uv_cb	5:4	rmw	**CB Undervoltage Filter Time** 11_B , 100 µs 10_B , 50 µs 01_B , 25 µs 00_B , 10 µs (default)
f_uv_vdh	3:2	rmw	**VDHP Undervoltage Filter Time** 11_B , 100 µs 10_B , 50 µs 01_B , 25 µs (default) 00_B , 10 µs
f_uv_vs	1:0	rmw	**Vs Undervoltage Filter Time** 11_B , 100 µs 10_B , 50 µs 01_B , 25 µs (default) 00_B , 10 µs

6.1.1.17 Overvoltage and VCC Filter Times

Ft_2

Overvoltage and VCC Filter Times

Address: 10_H

Reset value: 50_H

7	6	5	4	3	2	1	0
f_uv_vcc		**f_ov_vcc**		**f_ov_vdh**		**f_ov_vs**	
rmw		rmw		rmw		rmw	

Field	Bits	Type	Description
f_uv_vcc	7:6	rmw	**VCC Undervoltage Filter Time** 11_B , 100 µs 10_B , 50 µs 01_B , 25 µs (default) 00_B , 10 µs
f_ov_vcc	5:4	rmw	**VCC Overvoltage Filter Time** 11_B , 100 µs 10_B , 50 µs 01_B , 25 µs (default) 00_B , 10 µs
f_ov_vdh	3:2	rmw	**VDHP Overvoltage Filter Time** 11_B , 100 µs 10_B , 50 µs 01_B , 25 µs 00_B , 10 µs (default)
f_ov_vs	1:0	rmw	**Vs Overvoltage Filter Time** 11_B , 100 µs 10_B , 50 µs 01_B , 25 µs 00_B , 10 µs (default)

6.1.1.18 Overtemperature & Short Circuit Detection Filter Times

Ft_3 Address: 11_H

Overtemperature & Short Circuit Detection Filter Times Reset value: $0E_H$

7	6	5	4	3	2	1	0
f_ot_sd	**f_ot_w**		**f_bl_scd**			**f_fi_scd**	
rmw	rmw		rmw			rmw	

Field	Bits	Type	Description
f_ot_sd	7	rmw	**Overtemperature Shutdown Filter Time** 1_B , 50 µs 0_B , 10 µs (default)
f_ot_w	6:5	rmw	**Overtemperature Detection Filter Time** 11_B , 500 µs 10_B , 100 µs 01_B , 50 µs 00_B , 10 µs (default)
f_bl_scd	4:2	rmw	**Short Circuit Detection Blanking Time** 111_B , 15 µs 110_B , 10 µs 101_B , 5 µs 100_B , 3.5 µs 011_B , 2 µs (default) 010_B , 1.5 µs 001_B , 1.0 µs 000_B , 0.7 µs
f_fi_scd	1:0	rmw	**Short Circuit Detection Filter Time** 11_B , 5.8 µs 10_B , 3.8 µs (default) 01_B , 2.0 µs 00_B , 1.25 µs

6.1.1.19 Overcurrent Filter Time

Ft_4

Overcurrent Filter Time

Address: 12_H

Reset value: 02_H

7	6	5	4	3	2	1	0
Res						**f_oc_op**	
none						rmw	

Field	Bits	Type	Description
Res	7:2	none	**Reserved** 000000_B , default value. do not change.
f_oc_op	1:0	rmw	**Current Sense Amplifier Overcurrent Filter Time** 11_B , 10 µs 10_B , 5 µs (default) 01_B , 3 µs 00_B , 1.5 µs

6.1.1.20 Overcurrent Failure Modes

Fm_6 Address: 13_H

Overcurrent Failure Modes Reset value: 00_H

7	6	5	4	3	2	1	0
Res		**fm_oc_op3**		**fm_oc_op2**		**fm_oc_op1**	
none		rmw		rmw		rmw	

Field	Bits	Type	Description
Res	7:6	none	**Reserved** 00_B , default value. do not change.
fm_oc_op3	5:4	rmw	**Current Sense Amplifier 3 Overcurrent Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)
fm_oc_op2	3:2	rmw	**Current Sense Amplifier 2 Overcurrent Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)
fm_oc_op1	1:0	rmw	**Current Sense Amplifier 1 Overcurrent Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)

6.1.2 Control registers

6.1.2.1 Current Sense Amplifier 1&2 - Gain 1

Op_gain_1 Address: 20_H

Current Sense Amplifier 1&2 - Gain 1 Reset value: 33_H

7	6	5	4	3	2	1	0
Res	**op1_gain1**			**Res**	**op2_gain1**		
none	rw			none	rw		

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
op1_gain1	6:4	rw	**Current Sense Amplifier 1 - Gain 1** 111_B , 83.19 110_B , 38.13 101_B , 34.45 100_B , 30.81 011_B , 26.90 (default) 010_B , 23.35 001_B , 19.56 000_B , 15.71
Res	3	none	**Reserved** 0_B , default value. do not change.
op2_gain1	2:0	rw	**Current Sense Amplifier 2 - Gain 1** 111_B , 83.19 110_B , 38.13 101_B , 34.45 100_B , 30.81 011_B , 26.90 (default) 010_B , 23.35 001_B , 19.56 000_B , 15.71

6.1.2.2 Current Sense Amplifier 1&2 - Gain 2

Op_gain_2 Address: 21_H

Current Sense Amplifier 1&2 - Gain 2 Reset value: 55_H

7	6	5	4	3	2	1	0
Res	**op1_gain2**			**Res**	**op2_gain2**		
none	rw			none	rw		

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
op1_gain2	6:4	rw	**Current Sense Amplifier 1 - Gain 2** 111_B , 83.19 110_B , 38.13 101_B , 34.45 (default) 100_B , 30.81 011_B , 26.90 010_B , 23.35 001_B , 19.56 000_B , 15.71
Res	3	none	**Reserved** 0_B , default value. do not change.
op2_gain2	2:0	rw	**Current Sense Amplifier 2 - Gain 2** 111_B , 83.19 110_B , 38.13 101_B , 34.45 (default) 100_B , 30.81 011_B , 26.90 010_B , 23.35 001_B , 19.56 000_B , 15.71

6.1.2.3 Current Sense Amplifier 3 - Gain 1&2

Op_gain_3 Address: 22_H

Current Sense Amplifier 3 - Gain 1&2 Reset value: 53_H

7	6	5	4	3	2	1	0
Res	**op3_gain2**			**Res**	**op3_gain1**		
none	rw			none	rw		

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
op3_gain2	6:4	rw	**Current Sense Amplifier 3 - Gain 2** 111_B , 83.19 110_B , 38.13 101_B , 34.45 (default) 100_B , 30.81 011_B , 26.90 010_B , 23.35 001_B , 19.56 000_B , 15.71
Res	3	none	**Reserved** 0_B , default value. do not change.
op3_gain1	2:0	rw	**Current Sense Amplifier 3 - Gain 1** 111_B , 83.19 110_B , 38.13 101_B , 34.45 100_B , 30.81 011_B , 26.90 (default) 010_B , 23.35 001_B , 19.56 000_B , 15.71

6.1.2.4 Current Sense Amplifier Zero Current Offset

Op_0cl Address: 23_H

Current Sense Amplifier Zero Current Offset Reset value: $5F_H$

7	6	5	4	3	2	1	0
zcl		**ofs**					
rw		rw					

Field	Bits	Type	Description
zcl	7:6	rw	**Zero Current Output Voltage Offset** 11_B , Reserved 10_B , 2.5 V 01_B , 1.65 V (default) 00_B , Reserved
ofs	5:0	rw	**Zero Current Output Voltage Offset Fine Adjustment** 111111_B , Most positive offset adjustment 011111_B , No adjustment (default) 000000_B , Most negative offset adjustment

6.1.2.5 Current Sense Amplifier Configuration

op_con Address: 24_H

Current Sense Amplifier Configuration Reset value: 07_H

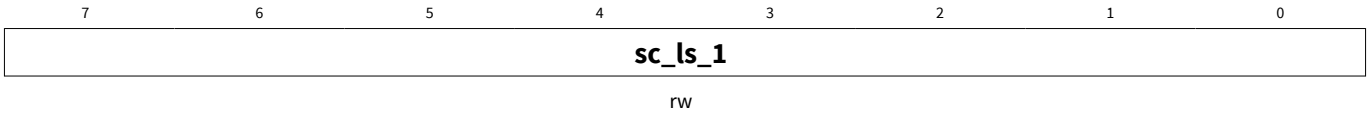
7	6	5	4	3	2	1	0
op1_cal	**op2_cal**	**op3_cal**	**Res**		**op1_cal_n**	**op2_cal_n**	**op3_cal_n**
rwc	rwc	rwc	none		rwc	rwc	rwc

Field	Bits	Type	Description
op1_cal	7	rwc	**CSA 1 Calibration start** 1_B , Set calibration (self clearing if completed) 0_B , No ongoing calibration (default)
op2_cal	6	rwc	**CSA 2 Calibration start** 1_B , Set calibration (self clearing if completed) 0_B , No ongoing calibration (default)
op3_cal	5	rwc	**CSA 3 Calibration start** 1_B , Set calibration (self clearing if completed) 0_B , No ongoing calibration (default)
Res	4:3	none	**Reserved** 00_B , default value. do not change.
op1_cal_n	2	rwc	**No CSA 1 Calibration start** 1_B , No ongoing calibration (default) 0_B , Set calibration (self clearing if completed)
op2_cal_n	1	rwc	**No CSA 2 Calibration start** 1_B , No ongoing calibration (default) 0_B , Set calibration (self clearing if completed)
op3_cal_n	0	rwc	**No CSA 3 Calibration start** 1_B , No ongoing calibration (default) 0_B , Set calibration (self clearing if completed)

6.1.2.6 Short Circuit Detection Threshold Low-side 1

Sc_ls_1 Address: 25_H

Short Circuit Detection Threshold Low-side 1 Reset value: $1A_H$

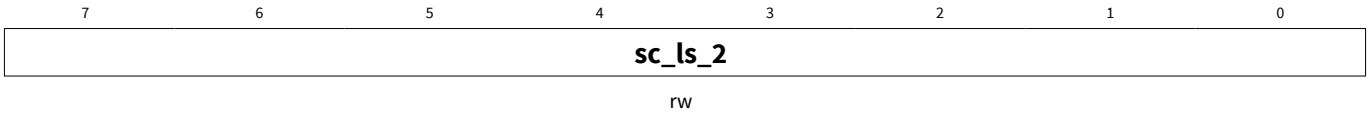


Field	Bits	Type	Description
sc_ls_1	7:0	rw	**Low-side 1 SCD Threshold (positive Two's Complement only)** [formula: (value)*1.215/104; unit: Volt] 01111111_B , SCD deactivated 01111110_B , 1.472 V - Maximum SCDL 00011010_B , 304 mV (default) 00000001_B , 11.7 mV - Minimum SCDL

6.1.2.7 Short Circuit Detection Threshold Low-side 2

Sc_ls_2 Address: 26_H

Short Circuit Detection Threshold Low-side 2 Reset value: $1A_H$

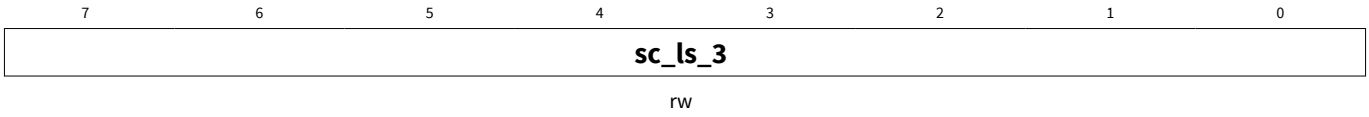


Field	Bits	Type	Description
sc_ls_2	7:0	rw	**Low-side 2 SCD Threshold (positive Two's Complement only)** [formula: (value)*1.215/104; unit: Volt] 01111111_B , SCD deactivated 01111110_B , 1.472 V - Maximum SCDL 00011010_B , 304 mV (default) 00000001_B , 11.7 mV - Minimum SCDL

6.1.2.8 Short Circuit Detection Threshold Low-side 3

Sc_ls_3 Address: 27_H

Short Circuit Detection Threshold Low-side 3 Reset value: $1A_H$

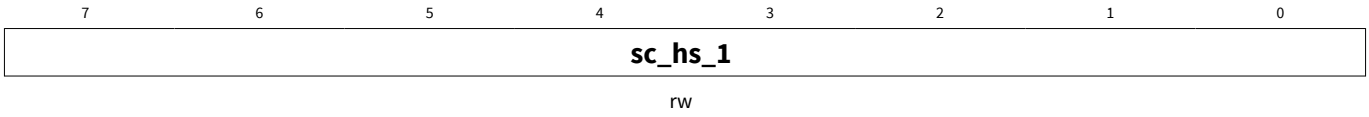


Field	Bits	Type	Description
sc_ls_3	7:0	rw	**Low-side 3 SCD Threshold (positive Two's Complement only)** [formula: (value)*1.215/104; unit: Volt] 01111111_B , SCD deactivated 01111110_B , 1.472 V - Maximum SCDL 00011010_B , 304 mV (default) 00000001_B , 11.7 mV - Minimum SCDL

6.1.2.9 Short Circuit Detection Threshold High-side 1

Sc_hs_1 Address: 28_H

Short Circuit Detection Threshold High-side 1 Reset value: $1A_H$

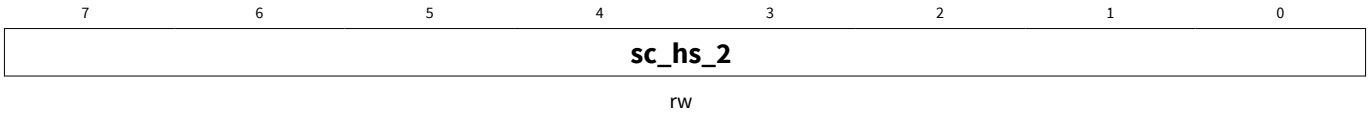


Field	Bits	Type	Description
sc_hs_1	7:0	rw	**High-side 1 SCD Threshold (positive Two's Complement only)** [formula: (value)*1.215/104; unit: Volt] 01111111_B , SCD deactivated 01111110_B , 1.472 V - Maximum SCDL 00011010_B , 304 mV (default) 00000001_B , 11.7 mV - Minimum SCDL

6.1.2.10 Short Circuit Detection Threshold High-side 2

Sc_hs_2 Address: 29_H

Short Circuit Detection Threshold High-side 2 Reset value: $1A_H$



Field	Bits	Type	Description
sc_hs_2	7:0	rw	**High-side 2 SCD Threshold (positive Two's Complement only)** [formula: (value)*1.215/104; unit: Volt] 01111111_B , SCD deactivated 01111110_B , 1.472 V - Maximum SCDL 00011010_B , 304 mV (default) 00000001_B , 11.7 mV - Minimum SCDL

6.1.2.11 Short Circuit Detection Threshold High-side 3

Sc_hs_3 Address: $2A_H$

Short Circuit Detection Threshold High-side 3 Reset value: $1A_H$

7	6	5	4	3	2	1	0
sc_hs_3							
rw							

Field	Bits	Type	Description
sc_hs_3	7:0	rw	**High-side 3 SCD Threshold (positive Two's Complement only)** [formula: (value)*1.215/104; unit: Volt] 01111111_B , SCD deactivated 01111110_B , 1.472 V - Maximum SCDL 00011010_B , 304 mV (default) 00000001_B , 11.7 mV - Minimum SCDL

6.1.2.12 Limp Home Activation and Half Bridge Deactivation

Li_ctr Address: $2B_H$

Limp Home Activation and Half Bridge Deactivation Reset value: $E8_H$

7	6	5	4	3	2	1	0
en_hb3	**en_hb2**	**en_hb1**	**en_limp**	**ex_limp**	**dis_hb3**	**dis_hb2**	**dis_hb1**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
en_hb3	7	rw	**Enable Half Bridge 3** 1_B , Output stages of half bridge 3 active (default) 0_B , Output stages of half bridge 3 external FET off, dedicated protection functions deactivated
en_hb2	6	rw	**Enable Half Bridge 2** 1_B , Output stages of half bridge 2 active (default) 0_B , Output stages of half bridge 2 external FET off, dedicated protection functions deactivated
en_hb1	5	rw	**Enable Half Bridge 1** 1_B , Output stages of half bridge 1 active (default) 0_B , Output stages of half bridge 1 external FET off, dedicated protection functions deactivated
en_limp	4	rw	**Limp home Mode Entry** 1_B , Enter 0_B , Exit (default)
ex_limp	3	rw	**Limp home Mode Exit** 1_B , Exit (default) 0_B , Enter
dis_hb3	2	rw	**Disable Half Bridge 3** 1_B , Output stages of half bridge 3 external FET off, dedicated protection functions deactivated 0_B , Output stages of half bridge 3 active (default)
dis_hb2	1	rw	**Disable Half Bridge 2** 1_B , Output stages of half bridge 2 external FET off, dedicated protection functions deactivated 0_B , Output stages of half bridge 2 active (default)
dis_hb1	0	rw	**Disable Half Bridge 1** 1_B , Output stages of half bridge 1 external FET off, dedicated protection functions deactivated 0_B , Output stages of half bridge 1 active (default)

6.1.2.13 Shift Phase Voltage Feedback and CSA Gain

Misc_ctr Address: $2C_H$

Shift Phase Voltage Feedback and CSA Gain Reset value: 00_H

7	6	5	4	3	2	1	0
sh_op_gain	**Res**			**art**		**Res**	**pfb**
rw	none			rw		none	rw

Field	Bits	Type	Description
sh_op_gain	7	rw	**Shift between the gain registers of the Current Sense Amplifier Gain** 1_B , Gain Setting opX_gain2 active 0_B , Gain Setting opX_gain1 active (default)
Res	6:4	none	**Reserved** 000_B , default value. do not change.
art	3:2	rw	**Phase Selection in Rectification Mode** 11_B , Reserved 10_B , Phase 3 selected 01_B , Phase 2 selected 00_B , Phase 1 selected (default)
Res	1	none	**Reserved** 0_B , default value. do not change.
pfb	0	rw	**Digital Phase Feedback Thresholds** 1_B , 50/50% 0_B , 80/25% (default)

6.1.2.14 Passive Rectification Threshold

art_tlp Address: $2D_H$

Passive Rectification Threshold Reset value: $F8_H$

Field	Bits	Type	Description
tl_art_p	7:0	rw	**Passive Rectification Threshold (Two's Complement only)** [formula: (value-1)*1.215/104; unit: Volt] 00000001_B , -0 V - Maximum value 00000000_B , -0.0117 V 11111000_B , -0.105 V (default) 10000001_B , -1.495 V - Minimum value 10000000_B , deactivated

6.1.2.15 Active Rectification Threshold

art_tla Address: $2E_H$

Active Rectification Threshold Reset value: 06_H

Field	Bits	Type	Description
tl_art_a	7:0	rw	**Active Rectification Threshold (Two's Complement only)** [formula: (value)*1.215/104; unit: Volt] 01111111_B , deactivated 01111110_B , 1.472 V - Maximum value 00000110_B , 0.070 V (default) 00000001_B , 0.0117 V 00000000_B , 0 V - Minimum value

6.1.2.16 Rectification Filter Time

art_fi

Rectification Filter Time

Address: $2F_H$

Reset value: 53_H

7	6	5	4	3	2	1	0
fi_art_tlp				**fi_art_tla**			
rw				rw			

Field	Bits	Type	Description
fi_art_tlp	7:4	rw	**Passive Rectification Filter Time** 1111_B , Maximum Filter Time 0101_B , Default Filter Time 0000_B , Minimum Filter Time
fi_art_tla	3:0	rw	**Active Rectification Filter Time** 1111_B , Maximum Filter Time 0011_B , Default Filter Time 0000_B , Minimum Filter Time

6.1.2.17 Rectification Accuracy

art_acc

Rectification Accuracy

Address: 30_H

Reset value: 21_H

7	6	5	4	3	2	1	0
acc_art_tlp			**Res**		**acc_art_tla**		
rw			none		rw		

Field	Bits	Type	Description
acc_art_tlp	7:5	rw	**Passive Rectification Accuracy** 111_B , Reserved7 110_B , Reserved6 101_B , Reserved5 100_B , High accuracy 011_B , Reserved3 010_B , Medium accuracy 001_B , Low accuracy (default) 000_B , Reserved0
Res	4:3	none	**Reserved** 00_B , default value. do not change.
acc_art_tla	2:0	rw	**Active Rectification Accuracy** 111_B , Reserved7 110_B , Reserved6 101_B , Reserved5 100_B , High accuracy 011_B , Reserved3 010_B , Medium accuracy 001_B , Low accuracy (default) 000_B , Reserved0

6.1.2.18 Rectification Mode entry

art_entry Address: 31_H

Rectification Mode entry Reset value: 80_H

7	6	5	4	3	2	1	0
art_dis	**Res**						**art_en**
rw	none						rw

Field	Bits	Type	Description
art_dis	7	rw	**Rectification Mode Disable** 1_B , Exit rectification mode (default) 0_B , Enter rectification mode
Res	6:1	none	**Reserved** 000000_B , default value. do not change.
art_en	0	rw	**Rectification Mode Enable** 1_B , Enter rectification mode 0_B , Exit rectification mode (default)

6.1.2.19 No Operation

nop Address: 32_H

No Operation Reset value: 00_H

7	6	5	4	3	2	1	0
nop							
rw							

Field	Bits	Type	Description
nop	7:0	rw	**No Operation** 00000000_B , default

6.1.2.20 Reverse Diode Measurement

Drev_mark Address: 33_H

Reverse Diode Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
Drev_acc		**hs3**	**hs2**	**hs1**	**ls3**	**ls2**	**ls1**
rw		rwc	rwc	rwc	rwc	rwc	rwc

Field	Bits	Type	Description
Drev_acc	7:6	rw	**Accuracy of Reverse Diode Measurement** 11_B , Reserved 3 10_B , High Accuracy 01_B , Medium Accuracy 00_B , Low Accuracy (default)
hs3	5	rwc	**High-side 3 Reverse Diode Measurement** 1_B , Enabled (self clearing after measurement completed) 0_B , Disabled (default)
hs2	4	rwc	**High-side 2 Reverse Diode Measurement** 1_B , Enabled (self clearing after measurement completed) 0_B , Disabled (default)
hs1	3	rwc	**High-side 1 Reverse Diode Measurement** 1_B , Enabled (self clearing after measurement completed) 0_B , Disabled (default)
ls3	2	rwc	**Low-side 3 Reverse Diode Measurement** 1_B , Enabled (self clearing after measurement completed) 0_B , Disabled (default)
ls2	1	rwc	**Low-side 2 Reverse Diode Measurement** 1_B , Enabled (self clearing after measurement completed) 0_B , Disabled (default)
ls1	0	rwc	**Low-side 1 Reverse Diode Measurement** 1_B , Enabled (self clearing after measurement completed) 0_B , Disabled (default)

6.1.2.21 Drain Source Measurement

Ds_mark Address: 34_H

Drain Source Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
Res		**hs3**	**hs2**	**hs1**	**ls3**	**ls2**	**ls1**
none		rwc	rwc	rwc	rwc	rwc	rwc

Field	Bits	Type	Description
Res	7:6	none	**Reserved** 00_B , default value. do not change.
hs3	5	rwc	**High-side 3 Drain Source Measurement** 1_B , Enabled (self clearing after measurement deactivated) 0_B , Disabled (default)
hs2	4	rwc	**High-side 2 Drain Source Measurement** 1_B , Enabled (self clearing after measurement deactivated) 0_B , Disabled (default)
hs1	3	rwc	**High-side 1 Drain Source Measurement** 1_B , Enabled (self clearing after measurement deactivated) 0_B , Disabled (default)
ls3	2	rwc	**Low-side 3 Drain Source Measurement** 1_B , Enabled (self clearing after measurement deactivated) 0_B , Disabled (default)
ls2	1	rwc	**Low-side 2 Drain Source Measurement** 1_B , Enabled (self clearing after measurement deactivated) 0_B , Disabled (default)
ls1	0	rwc	**Low-side 1 Drain Source Measurement** 1_B , Enabled (self clearing after measurement deactivated) 0_B , Disabled (default)

6.1.3 Self_test registers

6.1.3.1 Self Test Selection 1

Sel_st_1 Address: 35_H

Self Test Selection 1 Reset value: 00_H

7	6	5	4	3	2	1	0
st_uv_vcc	**st_scd_hs**	**st_scd_ls**	**st_uv_cb**	**Res**	**st_hs**	**st_ls**	**Res**
rw	rw	rw	rw	none	rwc	rwc	none

Field	Bits	Type	Description
st_uv_vcc	7	rw	**VCC Undervoltage Self Test** 1_B , Enable 0_B , Disable (default)
st_scd_hs	6	rw	**Short Circuit Detection at High-side Self Test** 1_B , Enable 0_B , Disable (default)
st_scd_ls	5	rw	**Short Circuit Detection at Low-side Self Test** 1_B , Enable 0_B , Disable (default)
st_uv_cb	4	rw	**CB Undervoltage Self Test** 1_B , Enable 0_B , Disable (default)
Res	3	none	**Reserved** 0_B , default value. do not change.
st_hs	2	rwc	**Drain Source Voltage Measurement High-side Self Test** 1_B , Enable (self clearing) 0_B , Disable (default)
st_ls	1	rwc	**Drain Source Voltage Measurement Low-side Self Test** 1_B , Enable (self clearing) 0_B , Disable (default)
Res	0	none	**Reserved** 0_B , default value. do not change.

6.1.3.2 Self Test Selection 2

Sel_st_2 Address: 36_H

Self Test Selection 2 Reset value: 00_H

7	6	5	4	3	2	1	0
Res	**en_op3_gt2**	**en_op3_gt1**	**en_op2_gt2**	**en_op2_gt1**	**en_op1_gt2**	**en_op1_gt1**	**en_vreg_op**
none	rw	rw	rw	rw	rw	rw	rwc

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
en_op3_gt2	6	rw	**Current Sense Amplifier 3 - Self-test of CSA3 gain test high voltage VSSC_GTIHV with gain register op3_gain2** 1_B , Enable 0_B , Disable (default)
en_op3_gt1	5	rw	**Current Sense Amplifier 3 - Self-test of CSA3 gain test low voltage VSSC_GTILV with gain register op3_gain1** 1_B , Enable 0_B , Disable (default)
en_op2_gt2	4	rw	**Current Sense Amplifier 2 - Self-test of CSA2 gain test high voltage VSSC_GTIHV with gain register op2_gain2** 1_B , Enable 0_B , Disable (default)
en_op2_gt1	3	rw	**Current Sense Amplifier 2 - Self-test of CSA2 gain test low voltage VSSC_GTILV with gain register op2_gain1** 1_B , Enable 0_B , Disable (default)
en_op1_gt2	2	rw	**Current Sense Amplifier 1 - Self-test of CSA1 gain test high voltage VSSC_GTIHV with gain register op1_gain2** 1_B , Enable 0_B , Disable (default)
en_op1_gt1	1	rw	**Current Sense Amplifier 1 - Self-test of CSA1 gain test low voltage VSSC_GTILV with gain register op1_gain1** 1_B , Enable 0_B , Disable (default)
en_vreg_op	0	rwc	**Supply Voltage Measurement of Current Sense Amplifiers and Reference Buffer** 1_B , Enable 0_B , Disable (default)

6.1.3.3 Self Test Mode Entry

En_st

Self Test Mode Entry

Address: 37_H

Reset value: 80_H

7	6	5	4	3	2	1	0
dis_st	**Res**						**en_st**
rw	none						rw

Field	Bits	Type	Description
dis_st	7	rw	**Self Test Mode Disable** 1_B , Exit self test mode (default) 0_B , Enter self test mode
Res	6:1	none	**Reserved** 000000_B , default value. do not change.
en_st	0	rw	**Self Test Mode Enable** 1_B , Enter self test mode 0_B , Exit self test mode (default)

6.1.4 Read registers

6.1.4.1 Operation Mode Overview

Om_over Address: 40_H

Operation Mode Overview Reset value: 00_H

7	6	5	4	3	2	1	0
norm_m	**rect_m**	**err_m**	**soff_m**	**self_test_m**	**conf_lock**	**conf_m**	**idle_m**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
norm_m	7	r	**Normal Operation Mode (Motor Driving Mode) Active** 1_B , In Driving Mode 0_B , Not in Driving Mode
rect_m	6	r	**Normal Operation Mode (Rectification Mode) Active** 1_B , In Rectification Mode 0_B , Not in Rectification Mode
err_m	5	r	**Error Mode Active** 1_B , in Error Mode 0_B , Not in Error Mode
soff_m	4	r	**SOFF Mode Active** 1_B , In SOFF Mode 0_B , Not in SOFF Mode
self_test_m	3	r	**Self Test Mode Active** 1_B , in Self Test Mode 0_B , Not in Self Test Mode
conf_lock	2	r	**Configuration Lock Mode Active** 1_B , In Configuration Lock Mode 0_B , Not in Configuration Lock Mode
conf_m	1	r	**Configuration Mode Active** 1_B , In Configuration Mode 0_B , Not in Configuration Mode
idle_m	0	r	**Idle Mode Active** 1_B , In Idle Mode 0_B , Not in Idle Mode

6.1.4.2 Error Overview

Err_over Address: 41_H

Error Overview Reset value: 00_H

7	6	5	4	3	2	1	0
int12	**ext**	**outp**	**indiag**	**sd**	**scd**	**op**	**osf**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
int12	7	rc	**Internal Error** 1_B , Error set 0_B , No error
ext	6	rc	**External Error** 1_B , Error set 0_B , No error
outp	5	rc	**Output Pin Error** 1_B , Error set 0_B , No error
indiag	4	rc	**Input Pattern Violation Error** 1_B , Error set 0_B , No error
sd	3	rc	**Shutdown Error** 1_B , Error set 0_B , No error
scd	2	rc	**Short Circuit Error** 1_B , Error set 0_B , No error
op	1	rc	**Current Sense Amplifier Error** 1_B , Error set 0_B , No error
osf	0	rc	**Output Stage Feedback Error** 1_B , Error set 0_B , No error

6.1.4.3 Special Event Register

Ser Address: 42_H

Special Event Register Reset value: 00_H

7	6	5	4	3	2	1	0
err_ot_w	**lfw**	**ctrl_reg_invalid**	**gtm**	**apc_act**	**Res**	**limp_on**	**rom**
rc	rc	rc	r	r	none	r	rc

Field	Bits	Type	Description
err_ot_w	7	rc	**Overtemperature Detection** 1_B , Error set 0_B , No error
lfw	6	rc	**Latent Fault Warning** 1_B , Error set 0_B , No error
ctrl_reg_invalid	5	rc	**Error Correction of Control Register Failed** 1_B , Failed 0_B , No fail
gtm	4	r	**global test mode** 1_B , Entered 0_B , Not in global test mode
apc_act	3	r	**Phase Cut off Activation** 1_B , Activated 0_B , Deactivated
Res	2	none	**Reserved** 0_B , default value. do not change.
limp_on	1	r	**Limp Home Mode** 1_B , In Limp Home Mode 0_B , Not in Limp Home Mode (default)
rom	0	rc	**Reduced Operation Mode has occurred** 1_B , ROM occurred 0_B , No ROM occurred

6.1.4.4 Internal Errors 1

Err_i_1 Address: 43_H

Internal Errors 1 Reset value: 00_H

7	6	5	4	3	2	1	0
Res	**err_uv_cb**	**err_uv_reg5**	**err_uv_reg6**	**err_ov_reg6**	**err_uv_reg4**	**err_uv_vcc_rom**	**err_ov_reg1**
none	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
err_uv_cb	6	rc	**CB Undervoltage Detection Error** 1_B , Error set 0_B , No error
err_uv_reg5	5	rc	**Undervoltage Internal Regulator 5 Error for Reduced Operation Mode** 1_B , Error set 0_B , No error
err_uv_reg6	4	rc	**Undervoltage Internal Regulator 6 Error** 1_B , Error set 0_B , No error
err_ov_reg6	3	rc	**Overvoltage Internal Regulator 6 Error** 1_B , Error set 0_B , No error
err_uv_reg4	2	rc	**Undervoltage Internal Regulator 4 Error** 1_B , Error set 0_B , No error
err_uv_vcc_rom	1	rc	**Undervoltage External VCC for Reduced Operation Mode** 1_B , Error set 0_B , No error
err_ov_reg1	0	rc	**Overvoltage Internal Regulator 1 Error** 1_B , Error set 0_B , No error

6.1.4.5 Internal Errors 2

Err_i_2 Address: 44_H

Internal Errors 2 Reset value: 00_H

7	6	5	4	3	2	1	0
err_ov_bs1	**err_ov_bs2**	**err_ov_bs3**	**err_cp1**	**err_cp2**	**err_uv_bs1**	**err_uv_bs2**	**err_uv_bs3**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
err_ov_bs1	7	rc	**High-side Buffer Capacitor 1 Overvoltage Detection Error** 1_B , Error set 0_B , No error
err_ov_bs2	6	rc	**High-side Buffer Capacitor 2 Overvoltage Detection Error** 1_B , Error set 0_B , No error
err_ov_bs3	5	rc	**High-side Buffer Capacitor 3 Overvoltage Detection Error** 1_B , Error set 0_B , No error
err_cp1	4	rc	**Charge Pump 1 Overload Error** 1_B , Error set 0_B , No error
err_cp2	3	rc	**Charge Pump 2 Overload Error** 1_B , Error set 0_B , No error
err_uv_bs1	2	rc	**High-side Buffer Capacitor 1 Undervoltage Detection Error** 1_B , Error set 0_B , No error
err_uv_bs2	1	rc	**High-side Buffer Capacitor 2 Undervoltage Detection Error** 1_B , Error set 0_B , No error
err_uv_bs3	0	rc	**High-side Buffer Capacitor 3 Undervoltage Detection Error** 1_B , Error set 0_B , No error

6.1.4.6 External Errors

Err_e

External Errors

Address: 45_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Res	**Res**	**err_ov_vcc**	**err_uv_vcc**	**err_uv_vs**	**err_ov_vs**	**err_uv_vdh**	**err_ov_vdh**
none	none	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
Res	6	none	**Reserved** 0_B , default value. do not change.
err_ov_vcc	5	rc	**VCC Overvoltage Detection Error** 1_B , Error set 0_B , No error
err_uv_vcc	4	rc	**VCC Undervoltage Detection Error** 1_B , Error set 0_B , No error
err_uv_vs	3	rc	**Vs Undervoltage Detection Error** 1_B , Error set 0_B , No error
err_ov_vs	2	rc	**Vs Overvoltage Detection Error** 1_B , Error set 0_B , No error
err_uv_vdh	1	rc	**VDHP Undervoltage Detection Error** 1_B , Error set 0_B , No error
err_ov_vdh	0	rc	**VDHP Overvoltage Detection Error** 1_B , Error set 0_B , No error

6.1.4.7 Shutdown Errors

Err_sd Address: 46_H

Shutdown Errors Reset value: 00_H

7	6	5	4	3	2	1	0
sd_ot	**sd_ov_vs**	**Res**	**sd_uv_cb**	**sd_clkfail**	**sd_ov_cp**	**sd_cp1**	**sd_ddp_stuck**
rc	rc	none	rc	rc	rc	rc	rc

Field	Bits	Type	Description
sd_ot	7	rc	**Overtemperature Shutdown** 1_B , Error set 0_B , No error
sd_ov_vs	6	rc	**Vs Overvoltage Shutdown** 1_B , Error set 0_B , No error
Res	5	none	**Reserved** 0_B , default value. do not change.
sd_uv_cb	4	rc	**CB Undervoltage Shutdown** 1_B , Error set 0_B , No error
sd_clkfail	3	rc	**Internal Clock Supervision Shutdown** 1_B , Error set 0_B , No error
sd_ov_cp	2	rc	**Charge Pump Overvoltage Shutdown at Pin CB or Pin CH2-CL2** 1_B , Error set 0_B , No error
sd_cp1	1	rc	**Vs Path Charge Pump Input Overload** 1_B , Error set 0_B , No error
sd_ddp_stuck	0	rc	**Digital Driving Path Stucked Shutdown** 1_B , Error set 0_B , No error

6.1.4.8 Short Circuit Errors

Err_scd Address: 47_H

Short Circuit Errors Reset value: 00_H

7	6	5	4	3	2	1	0
err_scd_hs1	**err_scd_hs2**	**err_scd_hs3**	**err_scd_ls1**	**err_scd_ls2**	**err_scd_ls3**	**Res**	
rc	rc	rc	rc	rc	rc	none	

Field	Bits	Type	Description
err_scd_hs1	7	rc	**Short Circuit Detection at High-side 1** 1_B , Error set 0_B , No error
err_scd_hs2	6	rc	**Short Circuit Detection at High-side 2** 1_B , Error set 0_B , No error
err_scd_hs3	5	rc	**Short Circuit Detection at High-side 3** 1_B , Error set 0_B , No error
err_scd_ls1	4	rc	**Short Circuit Detection at Low-side 1** 1_B , Error set 0_B , No error
err_scd_ls2	3	rc	**Short Circuit Detection at Low-side 2** 1_B , Error set 0_B , No error
err_scd_ls3	2	rc	**Short Circuit Detection at Low-side 3** 1_B , Error set 0_B , No error
Res	1:0	none	**Reserved** 00_B , default value. do not change.

6.1.4.9 Input Pattern Violations

Err_indiag Address: 48_H

Input Pattern Violations Reset value: 00_H

7	6	5	4	3	2	1	0
err_ind_hs1	**err_ind_hs2**	**err_ind_hs3**	**err_ind_ls1**	**err_ind_ls2**	**err_ind_ls3**	**Res**	
rc	rc	rc	rc	rc	rc	none	

Field	Bits	Type	Description
err_ind_hs1	7	rc	**Input Pattern Violation at IH1_N** 1_B , Error set 0_B , No error
err_ind_hs2	6	rc	**Input Pattern Violation at IH2_N** 1_B , Error set 0_B , No error
err_ind_hs3	5	rc	**Input Pattern Violation at IH3_N** 1_B , Error set 0_B , No error
err_ind_ls1	4	rc	**Input Pattern Violation at IL1** 1_B , Error set 0_B , No error
err_ind_ls2	3	rc	**Input Pattern Violation at IL2** 1_B , Error set 0_B , No error
err_ind_ls3	2	rc	**Input Pattern Violation at IL3** 1_B , Error set 0_B , No error
Res	1:0	none	**Reserved** 00_B , default value. do not change.

6.1.4.10 Output Stage Feedback Errors

Err_osf Address: 49_H

Output Stage Feedback Errors Reset value: 00_H

7	6	5	4	3	2	1	0
err_osf_hs3	**err_osf_hs2**	**err_osf_hs1**	**err_osf_ls3**	**err_osf_ls2**	**err_osf_ls1**	**Res**	
rc	rc	rc	rc	rc	rc	none	

Field	Bits	Type	Description
err_osf_hs3	7	rc	**Output Stage High-side 3 Feedback Error** 1_B , Error set 0_B , No error
err_osf_hs2	6	rc	**Output Stage High-side 2 Feedback Error** 1_B , Error set 0_B , No error
err_osf_hs1	5	rc	**Output Stage High-side 1 Feedback Error** 1_B , Error set 0_B , No error
err_osf_ls3	4	rc	**Output Stage Low-side 3 Feedback Error** 1_B , Error set 0_B , No error
err_osf_ls2	3	rc	**Output Stage Low-side 2 Feedback Error** 1_B , Error set 0_B , No error
err_osf_ls1	2	rc	**Output Stage Low-side 1 Feedback Error** 1_B , Error set 0_B , No error
Res	1:0	none	**Reserved** 00_B , default value. do not change.

6.1.4.11 SPI Communication and Configuration Errors

Err_spiconf Address: $4A_H$

SPI Communication and Configuration Errors Reset value: 00_H

7	6	5	4	3	2	1	0
Res	**conf_sig_invalid**	**conf_to**	**spi_add_invalid**	**err_spi_crc**	**err_spi_wd**	**err_spi_to**	**err_spi_frame**
none	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Res	7	none	**Reserved** 0_B , default value. do not change.
conf_sig_invalid	6	rc	**Configuration Signature Invalid** 1_B , Error set 0_B , No error
conf_to	5	rc	**Configuration Time-Out** 1_B , Error set 0_B , No error
spi_add_invalid	4	rc	**Invalid Address Access** 1_B , Error set 0_B , No error
err_spi_crc	3	rc	**SPI CRC Error** 1_B , Error set 0_B , No error
err_spi_wd	2	rc	**SPI watchdog Error** 1_B , Error set 0_B , No error
err_spi_to	1	rc	**SPI Time-out** 1_B , Error set 0_B , No error
err_spi_frame	0	rc	**SPI Frame Error** 1_B , Error set 0_B , No error

6.1.4.12 Current Sense Amplifiers 1 & 2 Errors

Err_op_12 Address: $4B_H$

Current Sense Amplifiers 1 & 2 Errors Reset value: 00_H

7	6	5	4	3	2	1	0
err_op2_calib	**err_op2_ov**	**err_op2_uv**	**err_oc_op2**	**err_op1_calib**	**err_op1_ov**	**err_op1_uv**	**err_oc_op1**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
err_op2_calib	7	rc	**Current Sense Amplifier 2 Calibration Failed** 1_B , Error set 0_B , No error
err_op2_ov	6	rc	**Current Sense Amplifier 2 Supply Overvoltage** 1_B , Error set 0_B , No error
err_op2_uv	5	rc	**Current Sense Amplifier 2 Supply Undervoltage** 1_B , Error set 0_B , No error
err_oc_op2	4	rc	**Current Sense Amplifier 2 Overcurrent** 1_B , Error set 0_B , No error
err_op1_calib	3	rc	**Current Sense Amplifier 1 Calibration Failed** 1_B , Error set 0_B , No error
err_op1_ov	2	rc	**Current Sense Amplifier 1 and VRO Buffer Supply Overvoltage** 1_B , Error set 0_B , No error
err_op1_uv	1	rc	**Current Sense Amplifier 1 and VRO Buffer Supply Undervoltage** 1_B , Error set 0_B , No error
err_oc_op1	0	rc	**Current Sense Amplifier 1 Overcurrent** 1_B , Error set 0_B , No error

6.1.4.13 Current Sense Amplifier 3

Err_op_3

Current Sense Amplifier 3

Address: $4C_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
Res				**err_op3_calib**	**err_op3_ov**	**err_op3_uv**	**err_oc_op3**
none				rc	rc	rc	rc

Field	Bits	Type	Description
Res	7:4	none	**Reserved** 0000_B , default value. do not change.
err_op3_calib	3	rc	**Current Sense Amplifier 3 Calibration Failed** 1_B , Error set 0_B , No error
err_op3_ov	2	rc	**Current Sense Amplifier 3 Supply Overvoltage** 1_B , Error set 0_B , No error
err_op3_uv	1	rc	**Current Sense Amplifier 3 Supply Undervoltage** 1_B , Error set 0_B , No error
err_oc_op3	0	rc	**Current Sense Amplifier 3 Overcurrent** 1_B , Error set 0_B , No error

6.1.4.14 Digital Output Pin Errors

Err_outp Address: $4D_H$

Digital Output Pin Errors Reset value: 00_H

7	6	5	4	3	2	1	0
Res			**err_outp_PFB3**	**err_outp_PFB2**	**err_outp_PFB1**	**err_outp_miso**	**err_outp_errn**
none			rc	rc	rc	rc	rc

Field	Bits	Type	Description
Res	7:5	none	**Reserved** 000_B , default value. do not change.
err_outp_PFB3	4	rc	**PFB3 Pin Shorted** 1_B , Error set 0_B , No error
err_outp_PFB2	3	rc	**PFB2 Pin Shorted** 1_B , Error set 0_B , No error
err_outp_PFB1	2	rc	**PFB1 Pin Shorted** 1_B , Error set 0_B , No error
err_outp_miso	1	rc	**MISO Pin Shorted** 1_B , Error set 0_B , No error
err_outp_errn	0	rc	**ERR_N Pin Shorted** 1_B , Error set 0_B , No error

6.1.4.15 Low-side 1 Drain Source Measurement

dsm_ls1 Address: $4E_H$

Low-side 1 Drain Source Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
dsm_ls1							
r							

Field	Bits	Type	Description
dsm_ls1	7:0	r	**Low-side 1 Drain Source Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.16 Low-side 2 Drain Source Measurement

dsm_ls2 Address: $4F_H$

Low-side 2 Drain Source Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
dsm_ls2							
r							

Field	Bits	Type	Description
dsm_ls2	7:0	r	**Low-side 2 Drain Source Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.17 Low-side 3 Drain Source Measurement

dsm_ls3 Address: 50_H

Low-side 3 Drain Source Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
dsm_ls3							
r							

Field	Bits	Type	Description
dsm_ls3	7:0	r	**Low-side 3 Drain Source Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.18 High-side 1 Drain Source Measurement

dsm_hs1 Address: 51_H

High-side 1 Drain Source Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
dsm_hs1							
r							

Field	Bits	Type	Description
dsm_hs1	7:0	r	**High-side 1 Drain Source Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.19 High-side 2 Drain Source Measurement

dsm_hs2 Address: 52_H

High-side 2 Drain Source Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
dsm_hs2							
r							

Field	Bits	Type	Description
dsm_hs2	7:0	r	**High-side 2 Drain Source Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.20 High-side 3 Drain Source Measurement

dsm_hs3 Address: 53_H

High-side 3 Drain Source Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
dsm_hs3							
r							

Field	Bits	Type	Description
dsm_hs3	7:0	r	**High-side 3 Drain Source Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.21 Low-side 1 Reverse Diode Measurement

Rdm_ls1 Address: 54_H

Low-side 1 Reverse Diode Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
rdm_ls1							
r							

Field	Bits	Type	Description
rdm_ls1	7:0	r	**Low-side 1 Reverse Diode Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.22 Low-side 2 Reverse Diode Measurement

Rdm_ls2 Address: 55_H

Low-side 2 Reverse Diode Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
rdm_ls2							
r							

Field	Bits	Type	Description
rdm_ls2	7:0	r	**Low-side 2 Reverse Diode Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.23 Low-side 3 Reverse Diode Measurement

Rdm_ls3 Address: 56_H

Low-side 3 Reverse Diode Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
rdm_ls3							
r							

Field	Bits	Type	Description
rdm_ls3	7:0	r	**Low-side 3 Reverse Diode Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.24 High-side 1 Reverse Diode Measurement

Rdm_hs1 Address: 57_H

High-side 1 Reverse Diode Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
rdm_hs1							
r							

Field	Bits	Type	Description
rdm_hs1	7:0	r	**High-side 1 Reverse Diode Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.25 High-side 2 Reverse Diode Measurement

Rdm_hs2 Address: 58_H

High-side 2 Reverse Diode Measurement Reset value: 00_H

7	6	5	4	3	2	1	0
rdm_hs2							
r							

Field	Bits	Type	Description
rdm_hs2	7:0	r	**High-side 2 Reverse Diode Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.26 High-side 3 Reverse Diode Measurement

Rdm_hs3 Address: 59_H

High-side 3 Reverse Diode Measurement Reset value: 00_H

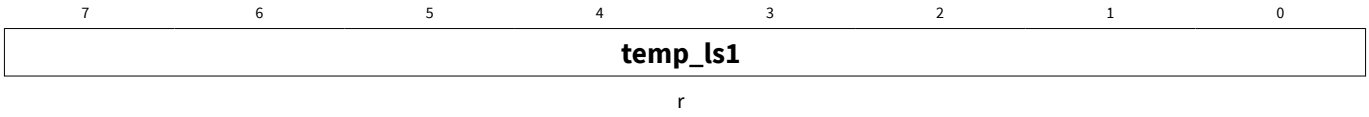
7	6	5	4	3	2	1	0
rdm_hs3							
r							

Field	Bits	Type	Description
rdm_hs3	7:0	r	**High-side 3 Reverse Diode Measurement Result (Two's Complement)** [formula: (value-1)*1.215/104; unit: Volt] 01111111_B , 1.472 V - Maximum value 10000000_B , -1.496 V - Minimum value

6.1.4.27 Low-side 1 Output Stage Temperature

temp_ls1 Address: $5A_H$

Low-side 1 Output Stage Temperature Reset value: 00_H

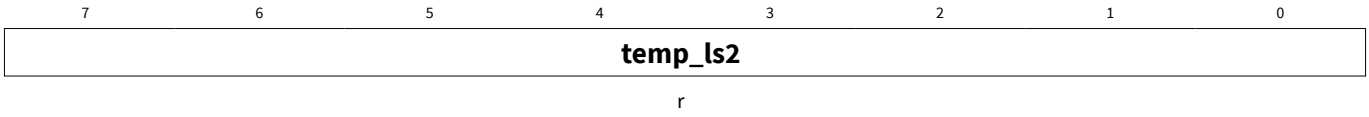


Field	Bits	Type	Description
temp_ls1	7:0	r	**Low-side 1 Output Stage Temperature** [formula: value*2.74*1.215/1.2/255; unit: Volt] 11111111_B , 2.774 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.28 Low-side 2 Output Stage Temperature

temp_ls2 Address: $5B_H$

Low-side 2 Output Stage Temperature Reset value: 00_H



Field	Bits	Type	Description
temp_ls2	7:0	r	**Low-side 2 Output Stage Temperature** [formula: value*2.74*1.215/1.2/255; unit: Volt] 11111111_B , 2.774 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.29 Low-side 3 Output Stage Temperature

temp_ls3 Address: $5C_H$

Low-side 3 Output Stage Temperature Reset value: 00_H

7	6	5	4	3	2	1	0
temp_ls3							
r							

Field	Bits	Type	Description
temp_ls3	7:0	r	**Low-side 3 Output Stage Temperature** [formula: value*2.74*1.215/1.2/255; unit: Volt] 11111111_B , 2.774 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.30 High-side 1 Output Stage Temperature

temp_hs1 Address: $5D_H$

High-side 1 Output Stage Temperature Reset value: 00_H

7	6	5	4	3	2	1	0
temp_hs1							
r							

Field	Bits	Type	Description
temp_hs1	7:0	r	**High-side 1 Output Stage Temperature** [formula: value*2.74*1.215/1.2/255; unit: Volt] 11111111_B , 2.774 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.31 High-side 2 Output Stage Temperature

temp_hs2 Address: $5E_H$

High-side 2 Output Stage Temperature Reset value: 00_H

7	6	5	4	3	2	1	0
temp_hs2							
r							

Field	Bits	Type	Description
temp_hs2	7:0	r	**High-side 2 Output Stage Temperature** [formula: value*2.74*1.215/1.2/255; unit: Volt] 11111111_B , 2.774 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.32 High-side 3 Output Stage Temperature

temp_hs3 Address: $5F_H$

High-side 3 Output Stage Temperature Reset value: 00_H

7	6	5	4	3	2	1	0
temp_hs3							
r							

Field	Bits	Type	Description
temp_hs3	7:0	r	**High-side 3 Output Stage Temperature** [formula: value*2.74*1.215/1.2/255; unit: Volt] 11111111_B , 2.774 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.33 Window Watchdog Loop Counter

wwlc Address: 60_H

Window Watchdog Loop Counter Reset value: 00_H

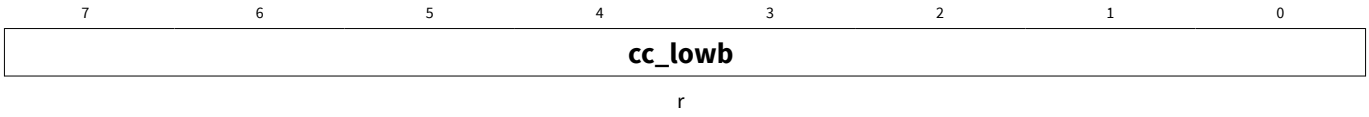
7	6	5	4	3	2	1	0
Res			**wwlc**				
none			r				

Field	Bits	Type	Description
Res	7:5	none	**Reserved** 000_B , default value. do not change.
wwlc	4:0	r	**Window Watchdog Loop Counter** 10000_B , Maximum Value 00000_B , Minimum Value (default)

6.1.4.34 Watchdog Clock Counter 1

res_cc1 Address: 61_H

Watchdog Clock Counter 1 Reset value: 00_H



Field	Bits	Type	Description
cc_lowb	7:0	r	**clock counter window watchdog low byte** 11111111_B , Maximum Value 00000000_B , Minimum Value

6.1.4.35 Watchdog Clock Counter 2

res_cc2 Address: 62_H

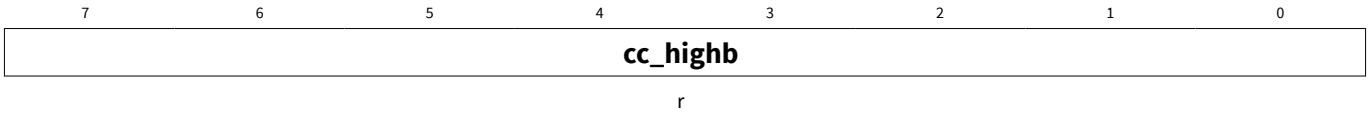
Watchdog Clock Counter 2 Reset value: 00_H

Field	Bits	Type	Description
cc_medb	7:0	r	**clock counter window watchdog medium byte** 11111111_B , Maximum Value 00000000_B , Minimum Value

6.1.4.36 Watchdog Clock Counter 3

res_cc3 Address: 63_H

Watchdog Clock Counter 3 Reset value: 00_H



Field	Bits	Type	Description
cc_highb	7:0	r	**clock counter window watchdog high byte** 11111111_B , Maximum Value 00000000_B , Minimum Value

6.1.4.37 VCC Measurement Result

res_vcc Address: 64_H

VCC Measurement Result Reset value: 00_H

Field	Bits	Type	Description
res_vcc	7:0	r	**VCC Measurement Result** [formula: value*5.48*1.215/1.2/255; unit: Volt] 11111111_B , 5.55 V - Maximum value 00000000_B , 0 V - Minimum Value

6.1.4.38 CB Measurement Result

res_cb Address: 65_H

CB Measurement Result Reset value: 00_H

7	6	5	4	3	2	1	0
res_cb							
r							

Field	Bits	Type	Description
res_cb	7:0	r	**CB Measurement Result** [formula: value*19.44/255; unit: Volt] 11111111_B , 19.44 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.39 Vs Measurement Result

res_vs Address: 66_H

Vs Measurement Result Reset value: 00_H

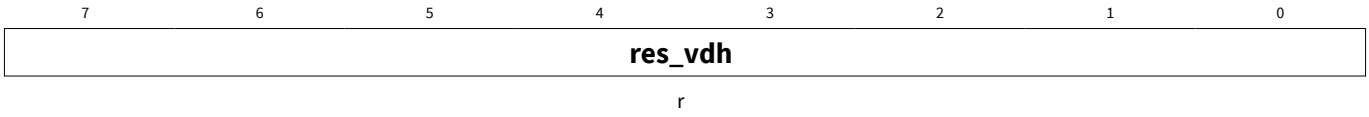
7	6	5	4	3	2	1	0
res_vs							
r							

Field	Bits	Type	Description
res_vs	7:0	r	**Vs Measurement Result** [formula: value*77.76/255; unit: Volt] 11111111_B , 77.76 V - Maximum value 00000000_B , 0 V - Minimum value

6.1.4.40 VDHP Measurement Result

res_vdh Address: 67_H

VDHP Measurement Result Reset value: 00_H



Field	Bits	Type	Description
res_vdh	7:0	r	**VDHP Measurement Result** [formula: value*77.76/255; unit: Volt] 11111111_B , 77.76 V - Maximum value 00000000_B , 0 V - Minimum value

7 Additional Components Recommendation

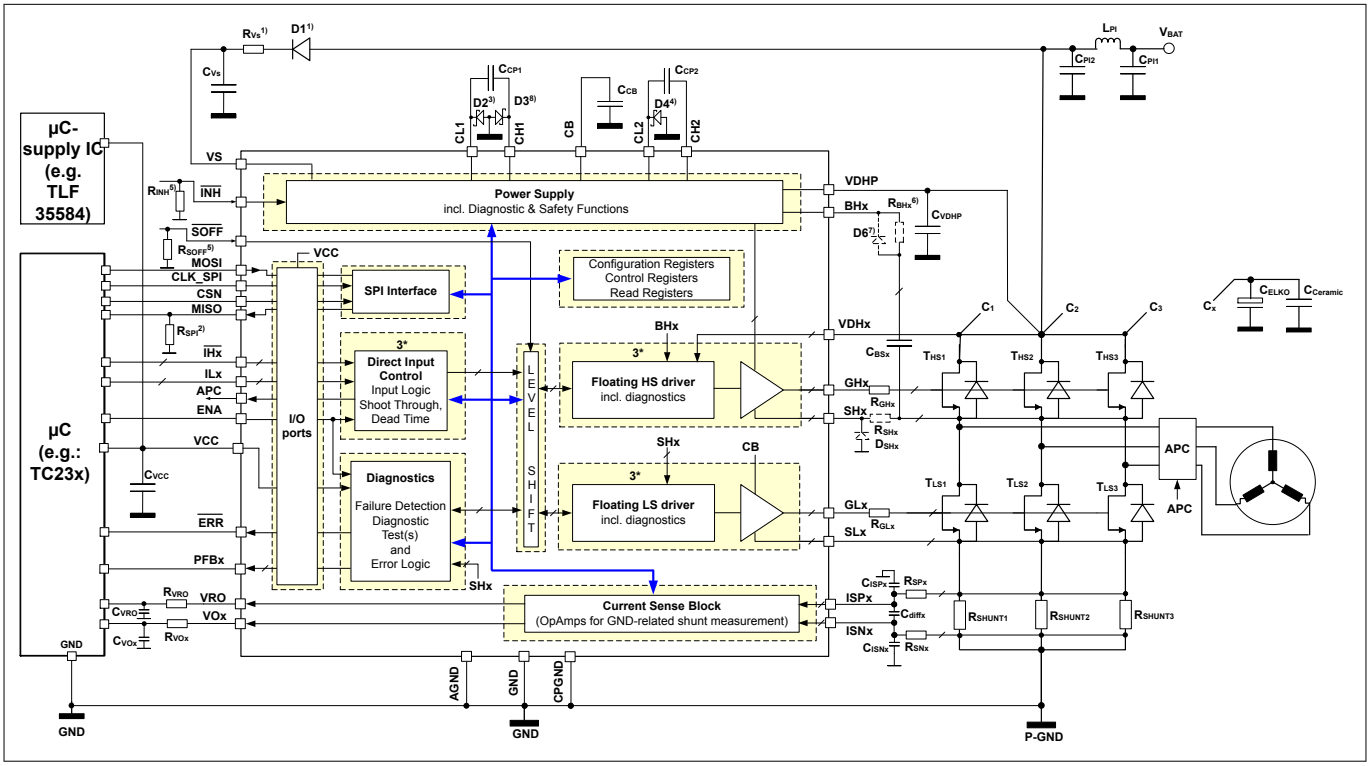


Figure 12 Simplified Recommended Application Circuit with Additional Components

Additional external components might be recommended to increase robustness. Please refer to TLE9183QK Data Sheet for layout guidelines and additional application hints.

1) Either R_{Vs} or D1 shall be implemented as reverse polarity protection and to filter voltage drops of the battery supply.

2) Referred to Data Sheet TLE9183QK High Level Output Voltage of Digital Output Pins termination to GND either via external resistor or internal µC port termination required.

3)D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D2 is not required with sufficient input filtering at the Vs pin.

4) D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data.

5) Pull-down resistor required to achieve low quiescent currents parameter under application condition

6) Resistor R_{BHx} is recommended in order to avoid minimum limit violations either at the parameter Absolute Maximum Ratings or Functional Range specified in the Data Sheet.

7) D6 is recommended if R_{BHx} is higher than 7 Ω.

8) D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D3 is not required with sufficient filtering at the Vs pin. In case D3 is not used a 100 kΩ pull down to GND at CL1 shall be placed.

Additionally, a protection circuit R_{SHx} of D_{SHx} avoids destruction of device in the case of negative transient higher than the maximum rating at pin SHx at the motor connection point. Special attention has to be paid if R_{SHx} is applied between the negative terminal of the bootstrap capacitor and the source of the external high-side FET. In this case the bootstrap capacitor charging pulses will generate a voltage drop via R_{SHx}. This voltage might provide sufficient gate source voltage for the high-side FET to turn on.

Revision History

Revision	Date	Changes
1.0	2019-07-31	User Manual created

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